Final Report
(Phase A)

Thin-Film Personal Communications and Telemetry System (TFPCTS)

For the Period
21 December 1964
to
21 December 1965

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National Aeronautics and Space Administration
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Submitted by

Melpar, Inc.
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Falls Church, Virginia 22046

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1. INTRODUCTION

This report (Final Report for Phase A) is submitted in compliance with Contract NAS 9-3924. Phase A of this contract was a research effort aimed at development of the necessary thin-film circuit elements to construct a "Thin-Film Personal Communications and Telemetry System (TFPCTS)" in monotronic form.

The work effort and research areas were defined and monitored through the use of a PERT chart. The chart was revised as research progressed until it evolved into the one presented in this report. In the first quarter the "High Frequency Substrate Investigation" was completed, and substrates were determined to be very satisfactory at frequencies up to 300 mc. In the second quarter the "Dielectric Investigation" was completed, and capacitors were also determined to be satisfactory in performance beyond the required 300 mc.

In the third quarter the "Inductor Investigation" and "High Magnetic Permeability Films" research efforts were concluded. Both of these investigations had been extended in both time and manpower to ensure that sufficient knowledge was obtained to properly evaluate their potential use in the TFPCTS. The inductors were developed to a point where they seemed practical and are included with the other passive components as available for use. Ferrite films were formed in vacuo, using standard vacuum deposition techniques for the first time under this contract. However, further development, beyond the scope of this contract, is necessary before this thin-film material can be optimized for circuit use. The chemical ferrite formed was reported in a NASA New Technology Brief.

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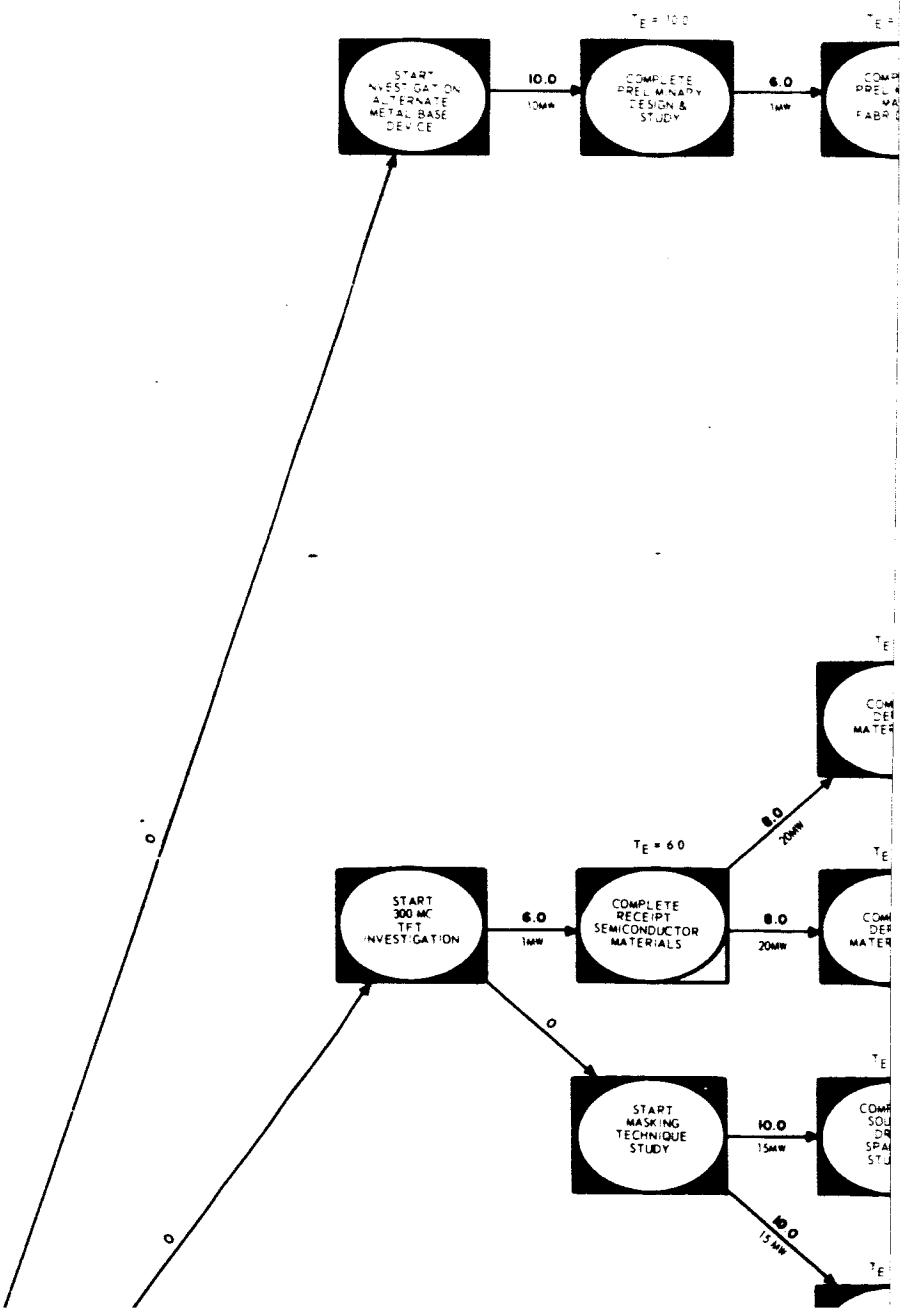

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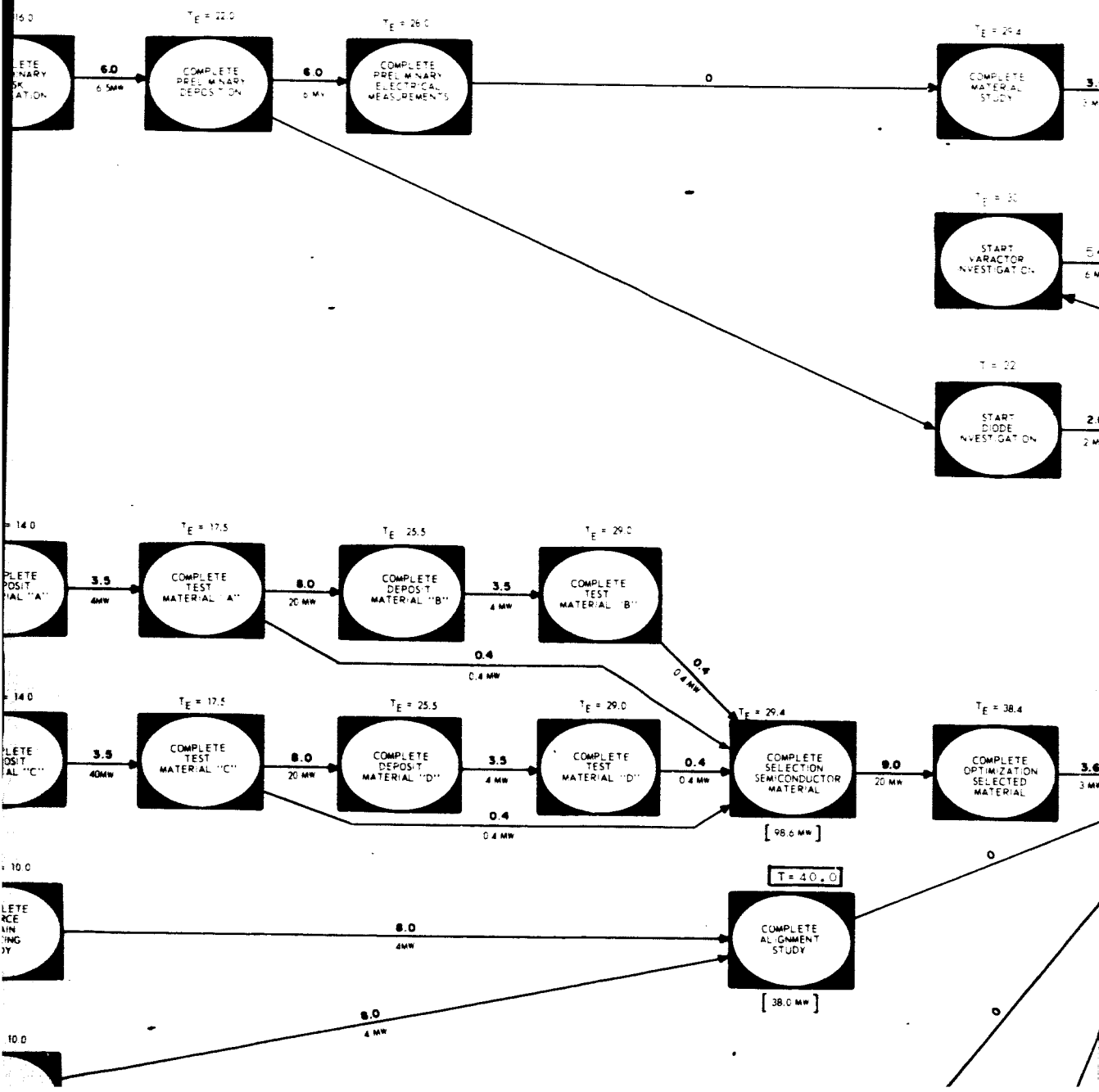

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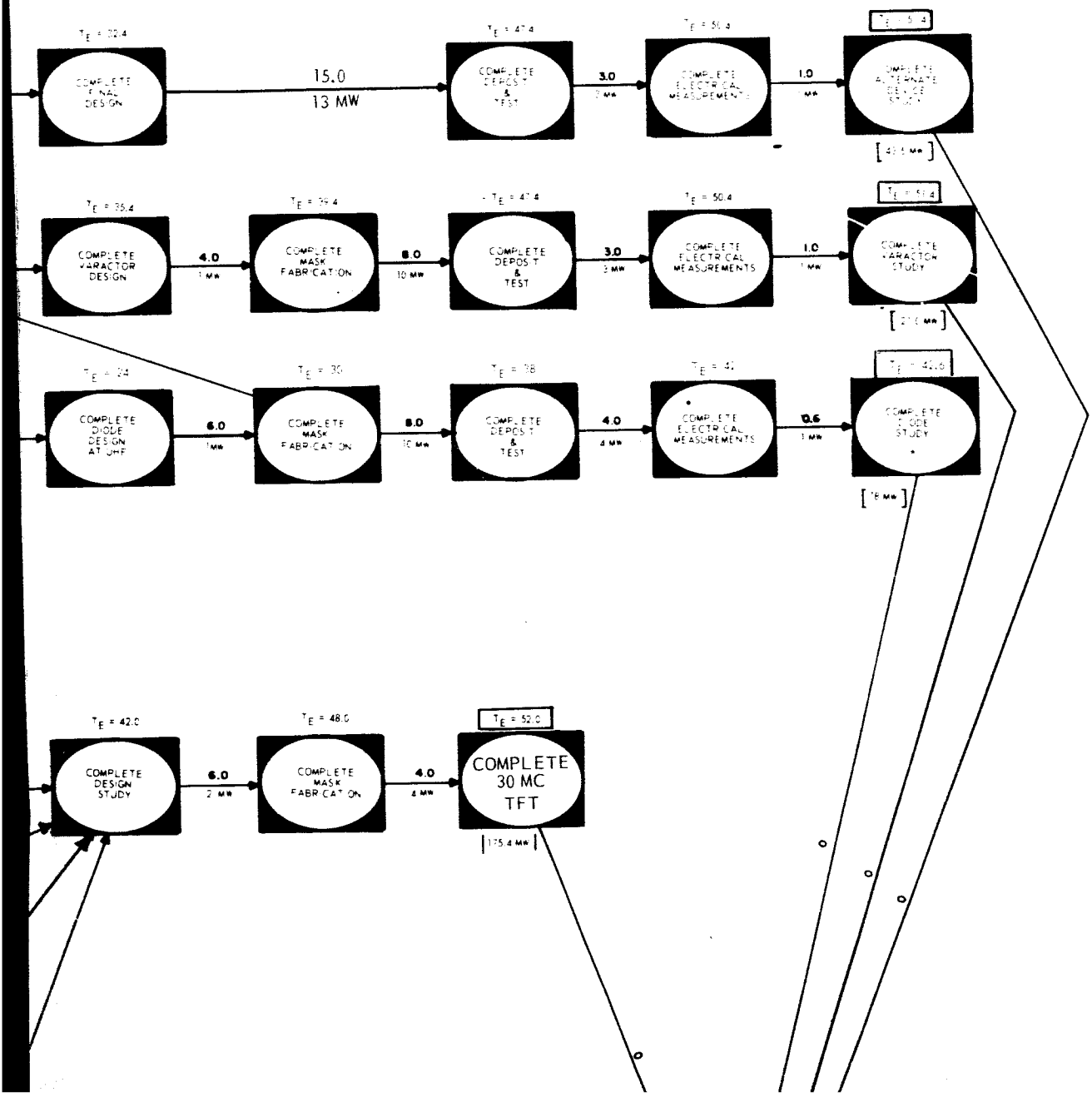

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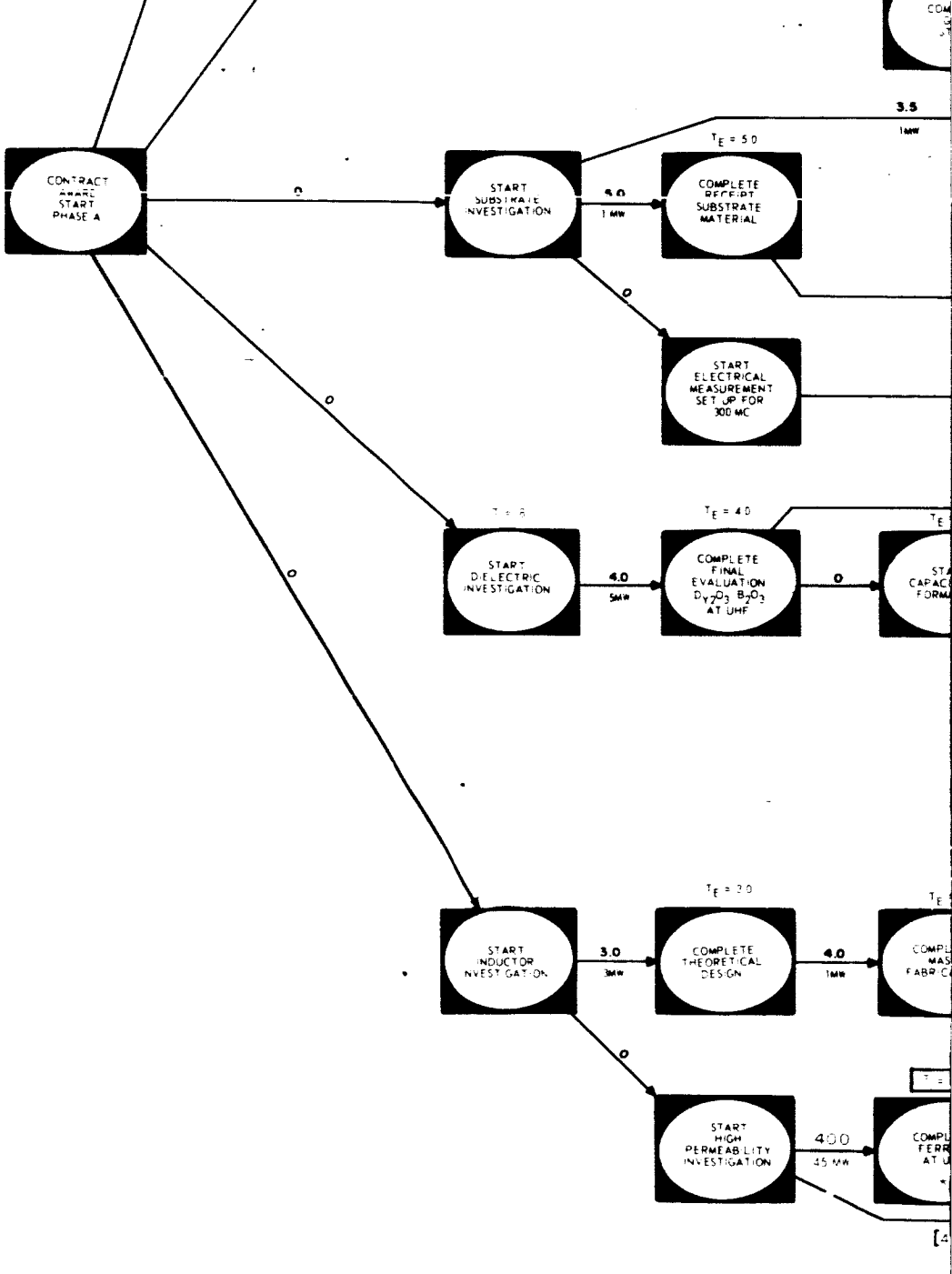

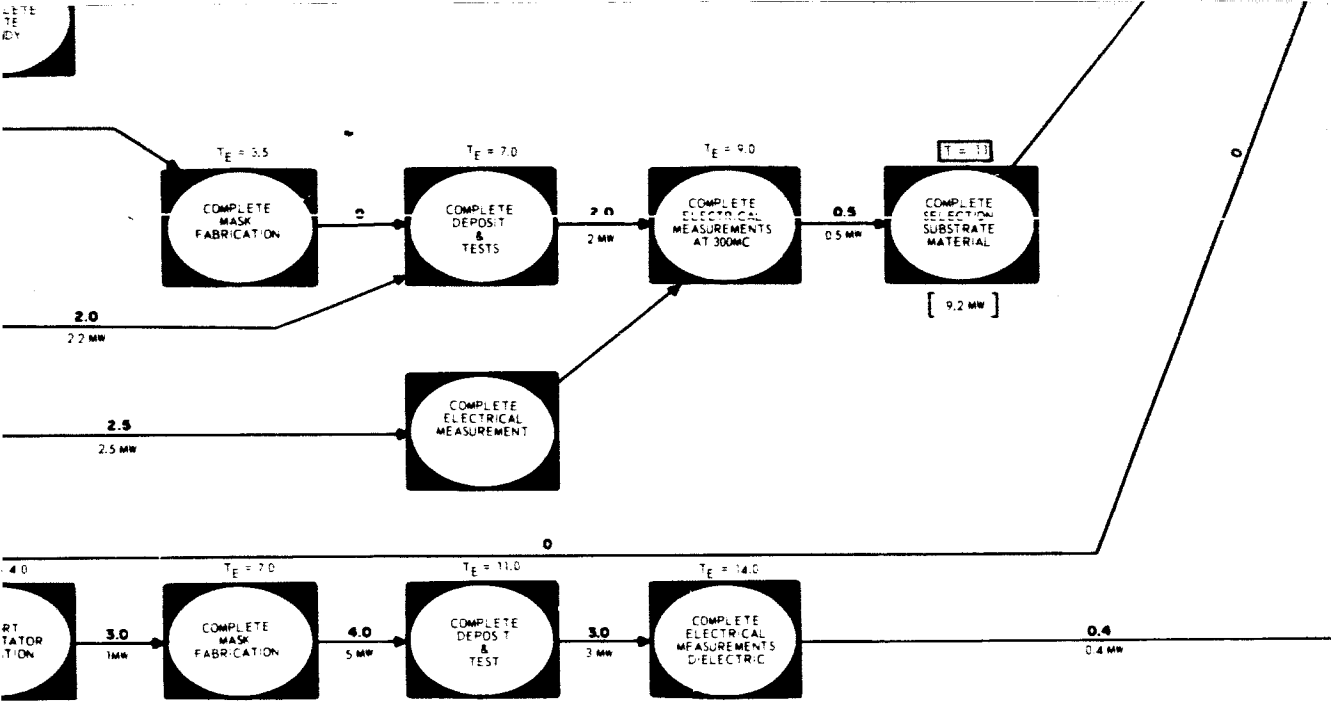

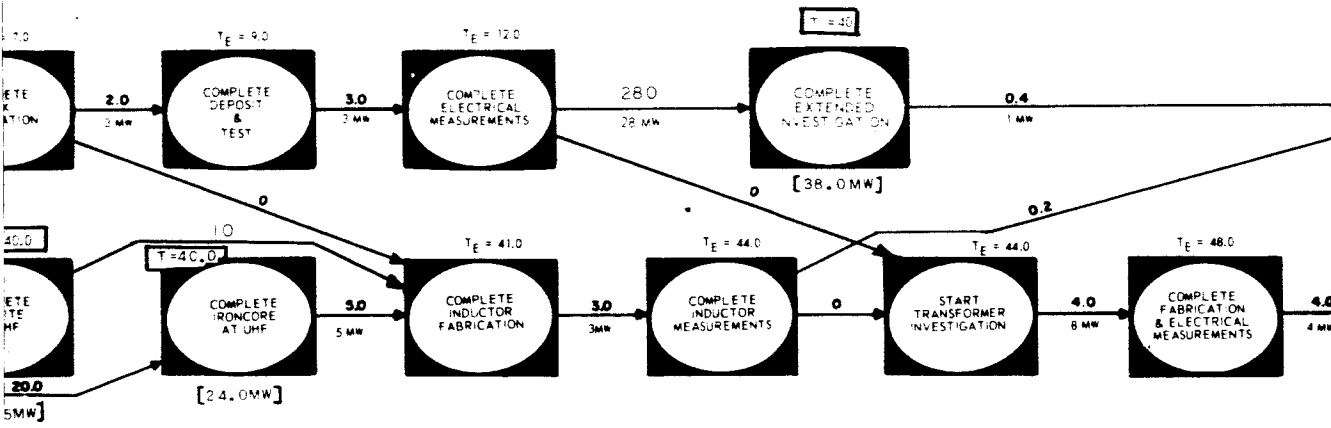

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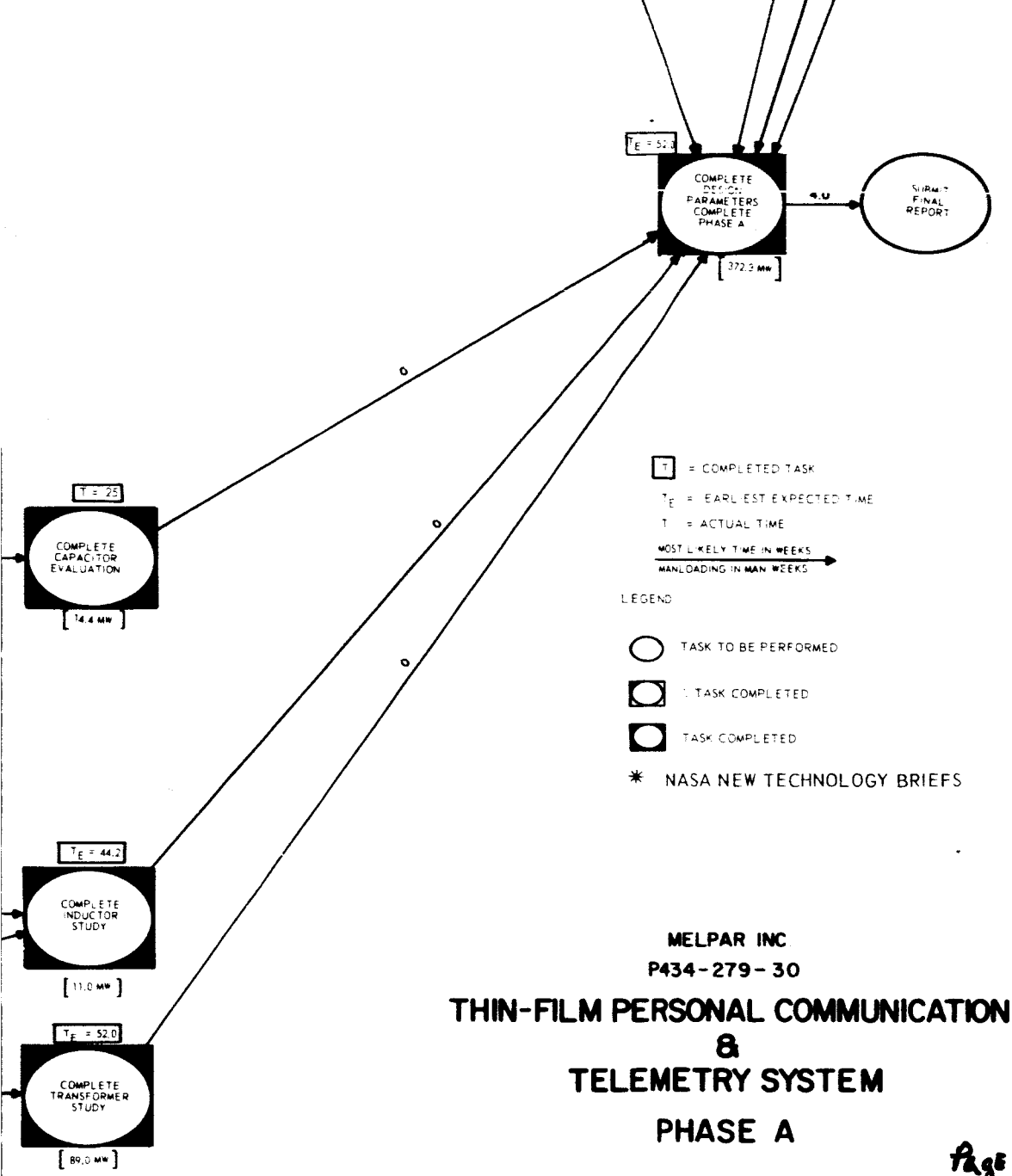

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THIN-FILM PERSONAL COMMUNICATION & TELEMETRY SYSTEM PHASE A

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One of the most exciting areas of research has been the "Metal Base Transistor." Early in the program a thin-film diode operating through the Schottky barrier mechanism for rectification was fabricated. This metal-semiconductor junction was so much better than the previously used thin-film diodes of the metal-dielectric-semiconductor barrier type that it was scheduled as the diode and varactor devices for this program. The metal-semiconductor junction also appears promising for high-frequency performance. A NASA New Technology Brief was submitted on this development. The metal base transistor and the diode were worked on concurrently. The formation of the diodes was very susceptible to the purity and present impurities of the semiconductors, and a great amount of effort has been expended in semiconductor evaluation. Before the close of this phase, however, some transistor action was obtained in a few transistors formed from these diodes.

"High-Frequency Thin-Film Triodes" is considered one of the most difficult research and development areas of the program. Special geometric configurations were developed for high-frequency TFT's. New methods for completing the devices with the narrowest possible gates were evolved. Special attention was given to selecting new semiconductor materials and optimizing both the new and the standard TFT semiconductor materials. The results at the end of this phase were that the TFT's had been improved an order of magnitude from 1 to 2 mc to 30 mc. However, the potential is still present for the many parameters to be combined in a fashion that will produce a 300-mc device sometime in the near future.

Some preliminary work, supported by Melpar, was carried out in anticipation of the circuit module work of Phase B.

This work is reported as "Circuit Design Considerations." The design concept for the TFPCTS has been completely breadboarded, using discrete components which were directly interchangeable with thin-film components where possible. Of this breadboarded TFPCTS, approximately 91% can be fabricated in monotronic form at the present time. Some items, such as the switches and large-value audio capacitors, will in all probability be more intelligently used in discrete form, but perhaps such items as a 300-mc TFT will be developed in sufficient time to be used, thus making this equipment "as completely thin-film as possible."

2. HIGH-FREQUENCY THIN-FILM TRIODES

2.1 General

During the past quarter, an increase in TFT transconductance (field effect mobility) was achieved due to what appears to be some improvement in deposition parameters and source material. Also, an analysis of the problems encountered with the high-frequency measurement techniques has been included. Efforts to achieve a high-frequency TFT were, in general, continued.

The format of this section includes the work of the fourth quarter, interspersed where applicable with the summary of phase A high-frequency TFT research. Also, a review of high-frequency TFT performance theory is included. This analysis was presented in the original proposals and is repeated here for the sake of completeness in the formal reports.

2.2 High-Frequency TFT Theory

The high-frequency response of a thin-film triode (TFT) can be limited primarily by three factors: (1) the effect of the device interelectrode capacitances (gain bandwidth product); (2) the effect of the carrier transit time; and (3) the effect of the gate RC time constant. The expressions for the cutoff frequency (fc) as a function of device material property and geometry can be derived for each of these limiting factors.

2.2.1 Interelectrode Capacitance (Gain Bandwidth Product)

To examine the effect of the gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}), the small-signal equivalent circuit (grounded source) of the TFT at high frequency will be analyzed. Such an equivalent circuit is shown in figure 1.

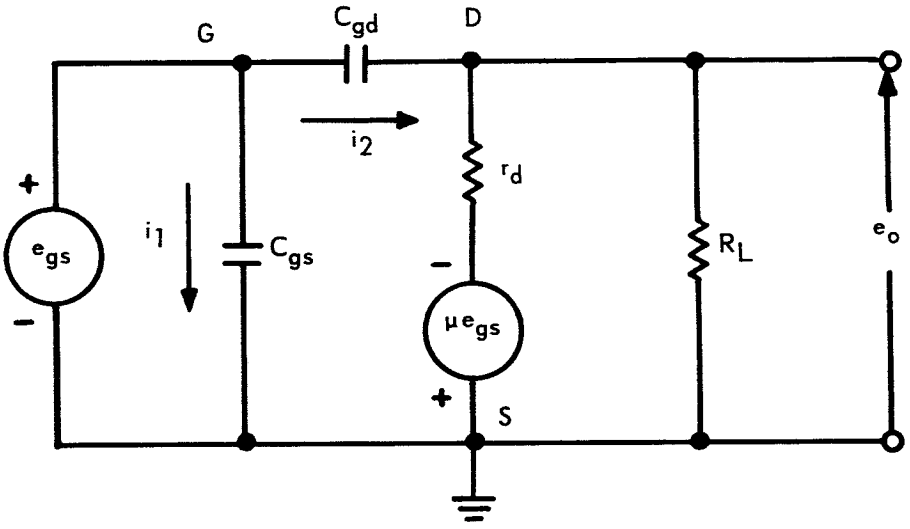


Figure 1. High-Frequency, Small-Signal Equivalent Circuit of TFT (Grounded Source)

Considering the circuit in figure 1, the input admittance can be written as

$$Y_{in} = \frac{i_{in}}{e_{in}} = \frac{i_1 + i_2}{e_{gs}} \tag{1}$$

where

$$i_1 = Y_{gs} e_{gs} \tag{2}$$

and

$$i_2 = (e_{gs} - e_o) Y_{gd} \tag{3}$$

Substituting equations (2) and (3) into equation (1) results in

$$Y_{in} = \frac{Y_{gs} e_{gs} + (e_{gs} - e_o) Y_{gd}}{e_{gs}} \tag{4}$$

The voltage gain of the device can be written as

$$A = \frac{e_o}{e_{gs}} \tag{5}$$

Substituting equation (5) into equation (4) yields

$$Y_{in} = Y_{gs} + (1 - A) Y_{gd} \tag{6}$$

Equation (6) can be written as

$$Y_{in} = jw\left[C_{gs} + (1 - A) C_{gd}\right] \tag{7}$$

Thus the input admittance is that from a capacitor between gate and source of magnitude

$$C_g = C_{gs} + (1 - A) C_{gd} \tag{8}$$

The equivalent circuit of a TFT amplifier "looking into" a succeeding stage is shown in figure 2. The effect of the "input" capacitance (C_g) of the following stage is to "shunt" the load resistor of the previous stage. The gain of the TFT with resistive load R_L can be written as

$$A_v = - g_m R_L \tag{9}$$

for $r_d \gg R_L$, where g_m is the device transconductance. Considering the effect of C_g, the load impedance can be written as

$$Z = \frac{\left(\frac{-j}{WC_{in}}\right)R_L}{R_L - j/WC_g} = \frac{R_L}{1 + jWC_g R_L} \tag{10}$$

and the gain of the amplifier can be written as

$$A_v = \frac{- g_m R_L}{1 + jWC_{in} R_L} \tag{11}$$

The useful bandwidth of an amplifier is defined as the frequency range for which the gain is greater than, or equal to, $\frac{1}{\sqrt{2}} |A_v|_{max}$, where $|A_v|_{max} = -g_m R_L$. The gain drops to $\frac{1}{\sqrt{2}} |A_v|_{max}$ when $WC_g R_L = 1$. Hence, the bandwidth of equation (11) is given by

$$B = \frac{1}{2\pi R_L C_g} \tag{12}$$

A figure of merit for defining the gain-bandwidth capabilities of the device is called the "gain-bandwidth product" and is defined as the maximum gain times the bandwidth. This product is given by

$$GBW = \frac{g_m}{2\pi C_g} \tag{13}$$

Equation (13) shows the effect of the interelectrode capacitances and the transconductance on the gain-bandwidth product.

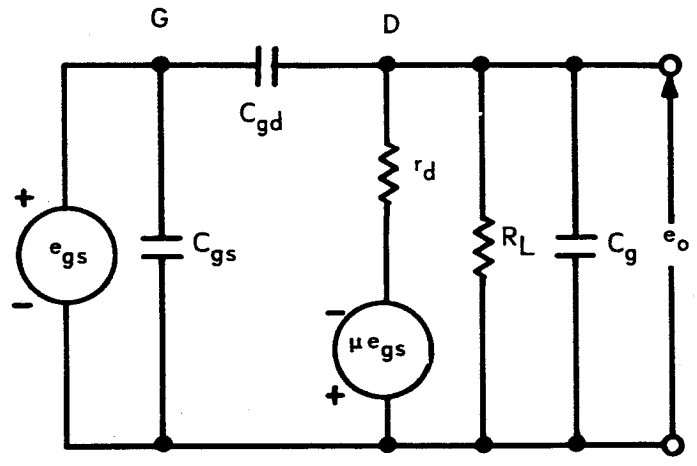


Figure 2. Equivalent Circuit of a TFT Amplfier "Looking Into" a Succeeding Stage

The derived expression[1] for the drain current as a function of gate voltage for a TFT is given by

$$I_d = \frac{\mu_d C_g}{L^2}\left[(V_g - V_o)\, V_d - \frac{V_d^2}{2}\right] \qquad (14)$$

where

$$V_o = \frac{qN_o}{C_g} = \text{voltage at the gate (relative to the source) required for the onset of drain current}$$

and

μ_d = drift mobility of the semiconductor

C_g = total gate capacitance

L = source-drain gap distance

V_g = gate voltage relative to the source

N_o = total number of initial charges in the semiconductor

V_d = drain voltage relative to the source

q = electronic charge

Equation (14) is valid only up to the onset of drain current saturation of the characteristic curves ($0 \leq V_d \leq \left[V_g - V_o\right]$). The drain current ($I_d$) is a maximum for a fixed value of V_g when $V_d = V_g - V_o$, and is given by

$$I_{d_{max}} = \frac{\mu_d C_g}{2L^2}(V_g - V_o)^2 \qquad (15)$$

From equation (15) the transconductance (g_m) of the device can be shown to be

$$g_m = \left[\frac{\partial I_{d_{max}}}{\partial V_g}\right]_{V_d = (V_g - V_o)} = \frac{\mu_d C_g}{L^2}(V_g - V_o) \qquad (16)$$

Substituting equation (16) into equation (13) results in

$$GBW = \frac{\mu_d (V_g - V_o)}{2\pi L^2} = \frac{\mu_d V_p}{2\pi L^2} \tag{17}$$

where V_p is the pinch-off voltage.

Equation (17) relates the gain bandwidth product to the drift mobility of the semiconductor, to the pinch-off voltage, and to the source-drain spacing.

2.2.2 Transit Time

If the carriers traversing the source-drain gap of a TFT cannot respond adequately to an impressed voltage, the device will not function.

The time required for a carrier in the semiconductor layer to traverse the source-drain gap of spacing L can be calculated as follows. The drift mobility (μ_d) of a carrier in the semiconductor can be defined as

$$\mu_d = \frac{v}{E} \tag{18}$$

where v is the carrier velocity and E is the electric field strength. The time (τ) required for a carrier to traverse gap spacing L can be written as

$$\tau = \frac{L}{v} \tag{19}$$

Combining equations (18) and (19) results in

$$\tau = \frac{L}{\mu_d E} \tag{20}$$

Assuming a constant electric field in the semiconductor, the electric field strength can be written as

$$E = \frac{V_d}{L} \tag{21}$$

where V_d is the applied drain voltage. Substituting equation (21) into equation (20) yields

$$\tau = \frac{L^2}{\mu_d V_d} \tag{22}$$

The frequency (fc) to which the carriers can no longer respond is given by

$$fc = \frac{1}{2\pi\tau} \tag{23}$$

Combining equations (22) and (23) yields

$$fc = \frac{\mu_d V_c}{2\pi L^2} \tag{24}$$

Equation (24) gives the theoretical frequency cut-off of the TFT due to transit time effects.

2.2.3 RC Time Constant

The frequency response of the TFT can also be estimated by considering the RC time constant of the charge control element.[2] To change the gate voltage, the gate capacity must be charged through the resistance of the channel. Assuming a wedge-shaped channel (figure 3), the gate capacity can be estimated to be

$$C_g = \frac{\left(\frac{k_1 \varepsilon_o LZ}{d}\right)\left(\frac{2k_2 \varepsilon_o LZ}{a}\right)}{\frac{k_1 \varepsilon_o LZ}{d} + \frac{2k_2 \varepsilon_o LZ}{a}} = \frac{2\varepsilon_o k_1 k_2 LZ}{k_1 a + 2k_2 d} \tag{25}$$

Assuming the height of the space-charge region (h) to be $\frac{a}{2}$ where

k_1 = dielectric constant of insulator material

k_2 = dielectric constant of semiconductor material

ε_o = permittivity of free space

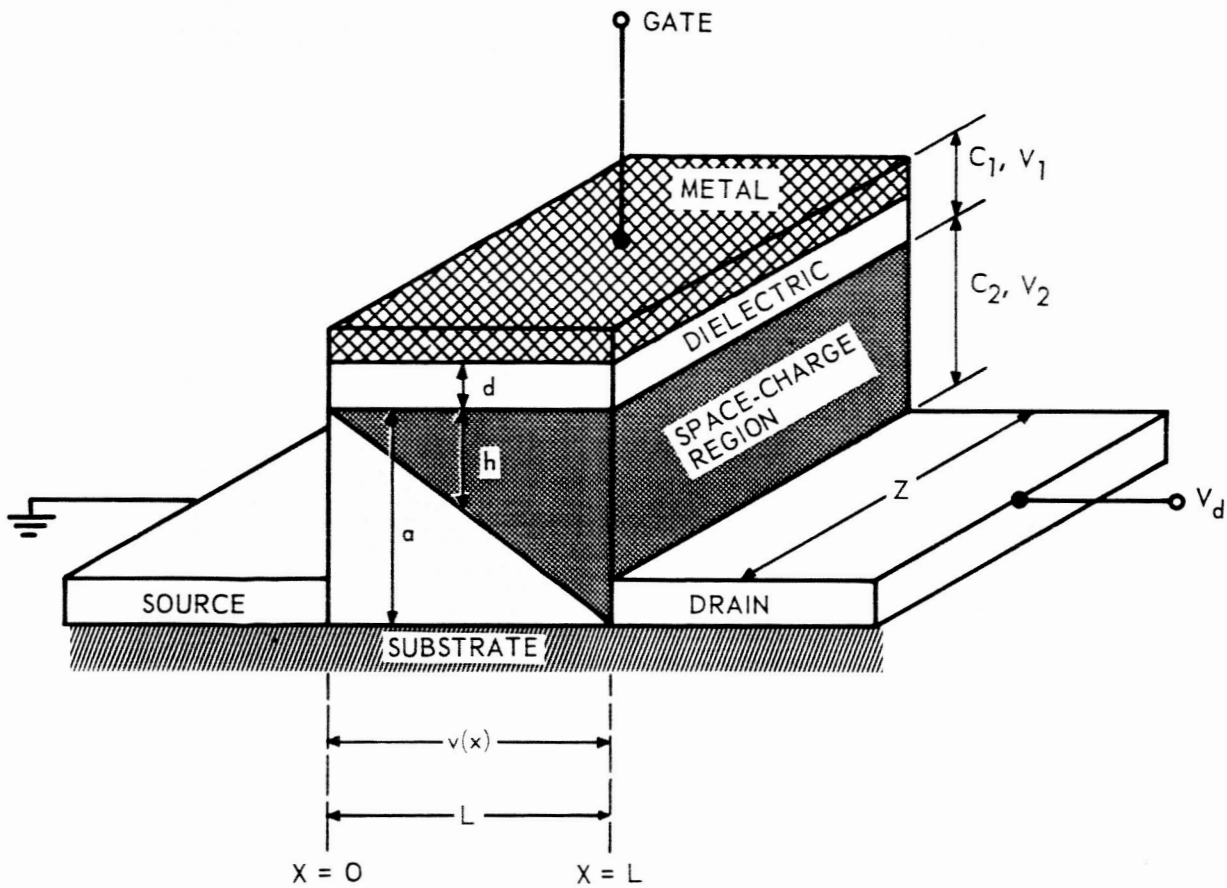


Figure 3. Geometrical Model of Operating TFT

a = thickness of semiconductor layer

d = thickness of insulating layer

L = source-drain spacing

Z = device width

On the average, this capacity charges through half the channel resistance; i.e.,

$$R = \frac{L}{Za\sigma} \tag{26}$$

where σ is the conductivity of the semiconductor channel. The limiting frequency can then be estimated as

$$fc = \frac{1}{2\pi RC} = \frac{a\sigma\,(k_1 a + 2k_2 d)}{4\pi\varepsilon_o k_1 k_2 L^2} \tag{27}$$

Assuming the drift mobility to be approximately equal to the Hall mobility, i.e.,

$$\mu_d \approx \mu_H = \frac{3\pi}{8}\,\frac{\sigma}{Nq} \tag{28}$$

one can write equation (27) as follows:

$$fc = \frac{(\frac{8}{3\pi})\, aNq\mu_d\,(k_1 a + 2k_2 d)}{(2\pi)\, 2k_1 k_2 \varepsilon_o L^2} \tag{29}$$

where N is the charge carrier density.

Considering the voltage division between the capacity formed by the dielectric material and the space-charge region, the relation between the potential at any point in the channel, v(x), and the height of the depletion layer at that point can be calculated to be[3]

$$v(x) = \frac{qNh(k_1 h + k_2 d)}{2k_1 k_2 \varepsilon_o} \tag{30}$$

where h is the height of the depletion layer at any point x in the semiconductor. Assuming, on the average, that $\overline{v(x)} = \frac{V_d}{2}$, since $v(x) = 0$ at $x = 0$ and $v(x) = V_d$ at $x = L$, then V_d can be written as

$$\bar{V}_d = \frac{qNh(k_1 h + k_2 d)}{k_1 k_2 \varepsilon_o} \tag{31}$$

Noting the assumption that, on the average, $h = \frac{a}{2}$, equation (31) can be written as

$$V_d = \frac{qNa(k_1 a + 2k_2 d)}{4k_1 k_2 \varepsilon_o} \tag{32}$$

Combining equations (29) and (32) yields the cut-off frequency due to RC time constant as

$$fc = \frac{8\mu_d V_d}{3\pi^2 L^2} \tag{33}$$

In general, equation (33) agrees with equations (17) and (24) except for the factor $\frac{3\pi}{16}$.

There is essential agreement between the frequency responses as estimated by gain-bandwidth product, transit time, and RC time constant considerations. The results of equations (17), (24), and (33) show the importance of a high semiconductor mobility, a small source-drain spacing, and a small area (narrow) gate electrode to high-frequency performance.

2.2.4 TFT Power Gain

Figure 4 shows a simplified equivalent circuit of a TFT. The series capacitance-resistance network shunting the input represents the effect of the channel. C_c represents the charge control capacity which must charge and discharge through channel resistance R_c. This is an approximation

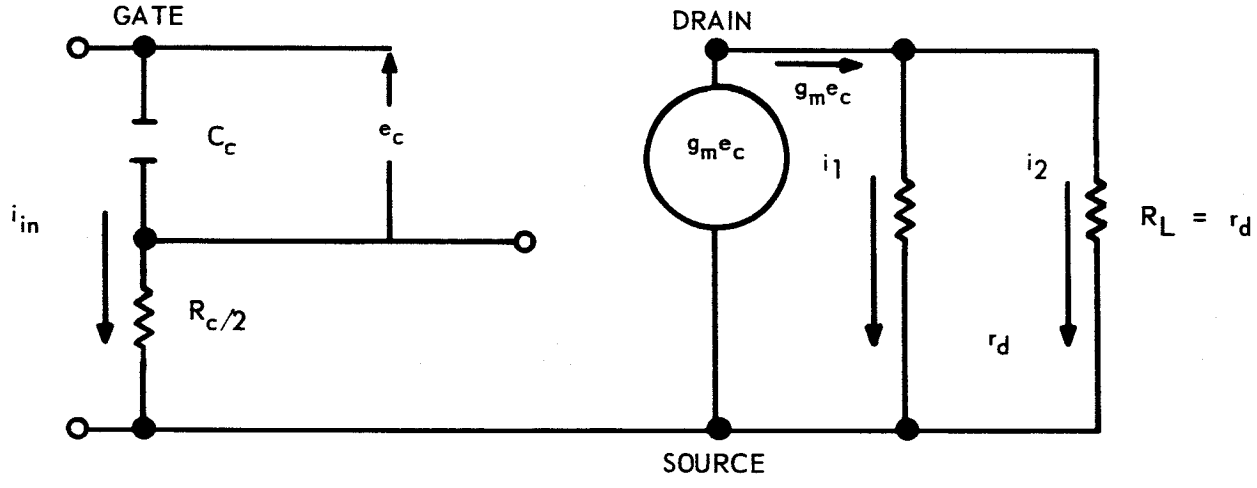


Figure 4. Simplified Equivalent Circuit for Power Gain Approximation

since C_c and R_c actually form a distributed parameter network. The voltage across C_c is the important modulation parameter, since C_c performs the charge control. The high-frequency response of the device is then a function of the input R_c time constant. This R_c characteristic is approximated by a lumped C_c charging and discharging through $R_c/2$.

For maximum amplifier power gain, impedance matching should be accomplished whenever possible. Assuming matched load conditions ($R_L - r_d$), the power gain of the TFT can be derived from the equivalent circuit of figure 4. The current delivered to the load is given by

$$i_2 = i_1 \frac{g_m e_c}{2} \tag{34}$$

and the power dissipated at the load is

$$P_{out} = i_2^2 r_d = \frac{(g_m e_c)^2}{4} r_d \tag{35}$$

The input current is related to the modulating voltage (e_c) by the relation

$$i_{in} = e_c \omega C_c \tag{36}$$

and the input power is given by

$$P_{in} = (i_{in})^2 \left(\frac{R_c}{2}\right) = (e_c \omega C_c)^2 \left(\frac{R_c}{2}\right) \tag{37}$$

The power gain of the device can be written as

$$P_{gain} = \frac{P_{out}}{P_{in}} \tag{38}$$

Substituting equations (35) and (37) into equation (38) results in

$$P_{gain} = \frac{g_m^2 r_d}{2(\omega C_c)^2 R_c} \tag{39}$$

The maximum power gain capability of a TFT is unusually large, due to the TFT input impedance (greater than 10^8 ohms) being great enough to almost completely inhibit gate current flow except through the interelectrode capacitances.

2.3 Semiconductor Film Experiments

Experiments with many semiconductor materials (in this contract and in other efforts) by this facility indicate that high mobility is only of value provided it can be achieved in thin films which exhibit sufficient field effect to be used in practical devices (TFT's).

Most of the III-V compounds, such as InSb and GaAs, in film form have been found to exhibit relatively high mobilities. These films, however, did not exhibit significant field effect. Very thin films (<500 A) that exhibited some field effect were tested but the thinner films exhibited low mobility (Melpar's 9th Quarterly Report, Bureau of Naval Weapons, Contract NOw 60-0362-c, 15 August 1962).

Based on experiments carried out under Bureau of Naval Weapons and Melpar programs, a decision was made to investigate films of a limited number of sulfides, selenides, and tellurides. Each material was initially studied. The forming techniques and property studies of each material were far too vast in number to allow a complete study.

During the course of this program, the following materials were studied and utilized as semiconductor films in TFT structures:

a. Cadmium sulfide (CdS).

b. Cadmium selenide (CdSe).

c. Cadmium sulfide-cadmium selenide mixture.

d. Tellurium (Te).

e. Cadmium telluride (undoped) (CdTe).

f. Cadmium telluride (indium doped) (CdTe).

g. Cadmium telluride (iodine doped) (CdTe).

h. Lead telluride (PbTe).

i. Silver telluride (Ag_2Te_3).

j. Bismuth selenide (Bi_2Se_3).

k. Bismuth telluride (Bi_2Te_3).

l. Manganese selenide (MnSe).

m. Manganese telluride (MnTe).

n. Tin sulfide (SnS).

These materials were deposited in small dual-vacuum chambers (figure 5). These small vacuum systems are located in a room where the relative humidity is held to 25% or less. Vacuums of 10^{-6} torr are achieved in less than 3 minutes. Deposits are usually made at initial vacuum pressures of $5x10^{-7}$ torr. Large roughing pumps (1398 Welsh) help to maintain relatively good vacuum ($5x10^{-6}$ torr) during any heavy outgassing of rapid deposits (i.e., CdSe).

Figure 6 is the basic vacuum chamber arrangement used in the evaporation of the materials.

The details of the evaporation techniques are given in Quarterly Report Nos. 1, 2, and 3 of this program.

Figure 7 is a block diagram of the Hall mobility measurement equipment, and figure 8 illustrates the use of the Tektronix curve tracer in displaying TFT electrical parameters. From the results of this effort, the following conclusions and points of interest were drawn:

a. Silver telluride films exhibited rather high mobilities (to 400 cm^2/volt second) for films of 2000 A. Higher mobilities were obtained on thicker films. Relatively poor field effect was observed in spite of good mobility measurements (Hall mobility).

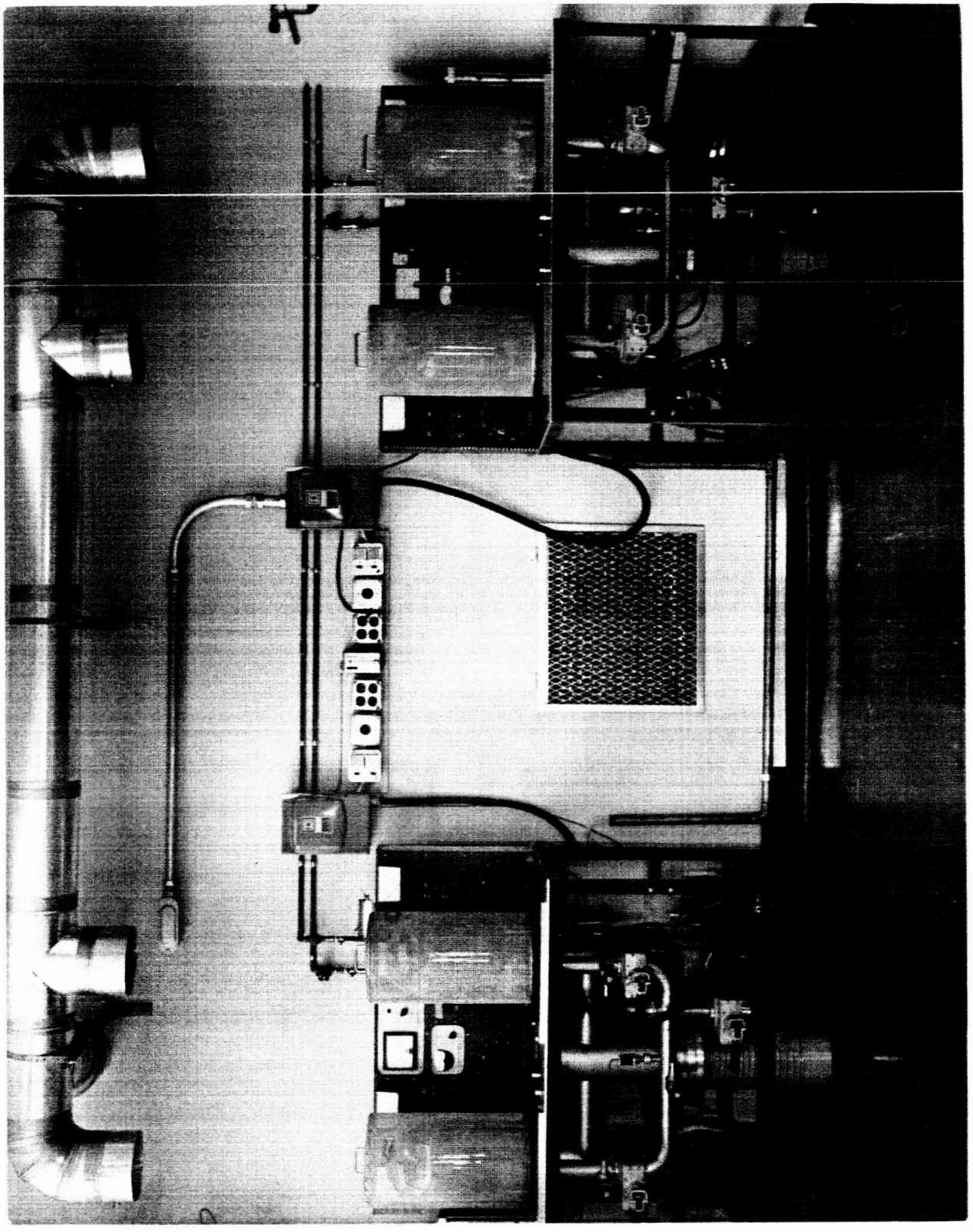


Figure 5. Dual 10-Inch Bell Jar Vacuum Systems

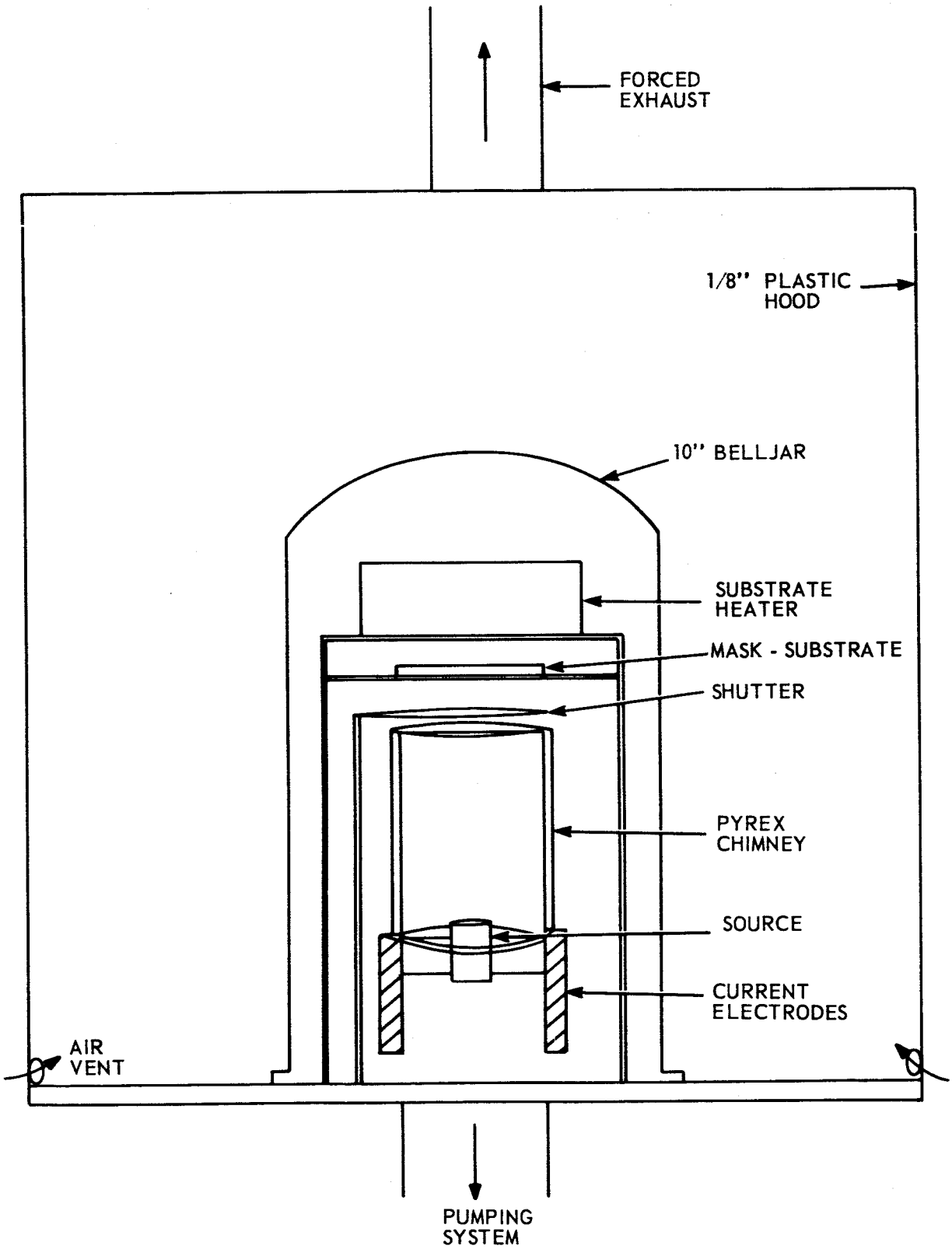
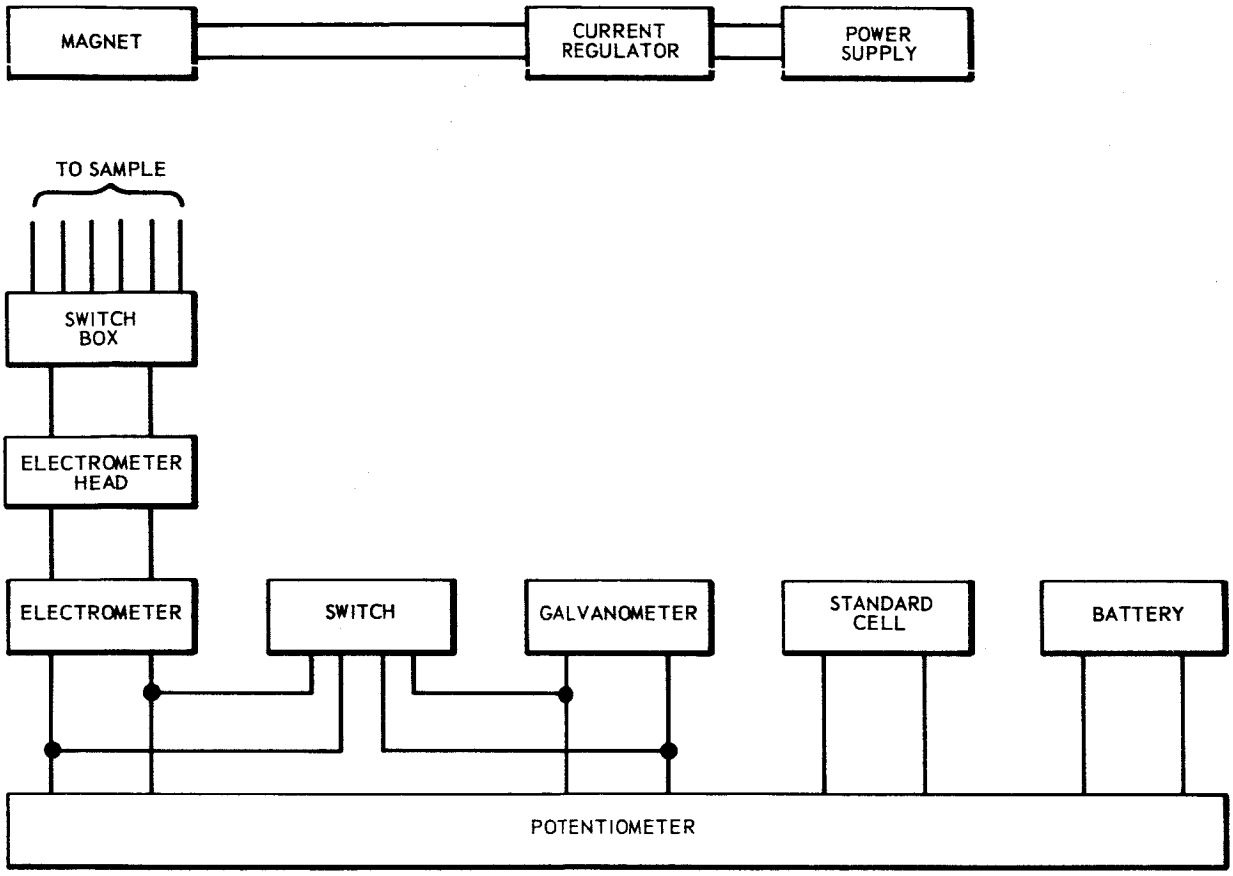


Figure 6. Enclosure and System Setup for Evaporations



POTENTIOMETER - LEEDS & NORTHRUP TYPE K-3
ELECTROMETER - CARY 31 VIBRATING REED
ELECTROMAGNETIC SYSTEM VARIAN MODEL
V-2301A (CURRENT REGULATOR) V-4004 (MAGNET)
V-2300A (POWER SUPPLY)

Figure 7. Block Diagram of Hall Mobility Measurement Equipment

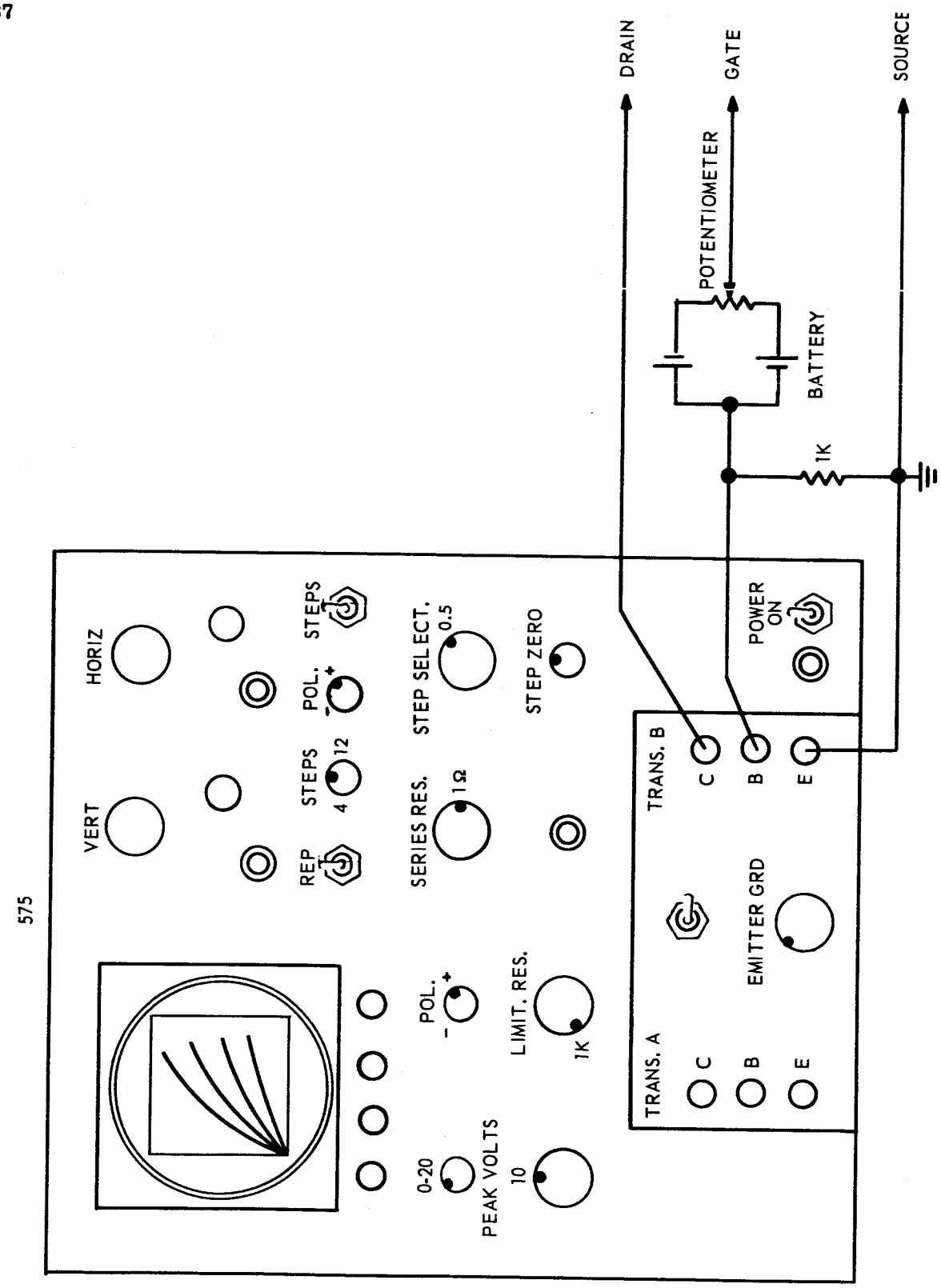


Figure 8. Use of Tektronic Transistor Curve Tracer in Testing TFT's

b. Except for CdTe and Ag_2Te_3, most tellurides were of poor mobility and exhibited poor device characteristics as compared to pure tellurium.

c. Cadmium telluride when doped with indium exhibited significant field effect and pinch-off (drain current saturation).

d. In view of the results obtained from device charactertistics, cadmium selenide and cadmium tellurium were chosen as the two materials which would exhibit the best characteristics in attempting to form high-frequency triodes.

Figures 9 through 19 exhibit typical device characteristics of TFT's utilizing some of the various semiconductor films listed. Equation (13) (an approximate formula for the calculation of "gain-bandwidth product") indicates the importance of a large transconductance (gm) for high frequency.

Work carried out during the fourth quarter of this program resulted in improvements in device transconductance values. Figure 19 shows transconductance values in excess of 25,000 micro-mhos for both a CdSe and a Te device. This improvement of transconductance did not come as a result of decreased source-drain spacing (5 microns by 100 mils). It appears that some improvement in deposition parameters and source material used is the reason. These latter results are presently being studied for indications as to why this increase of transconductance was achieved in spite of general deposition parameters being held to similar techniques used in the past.

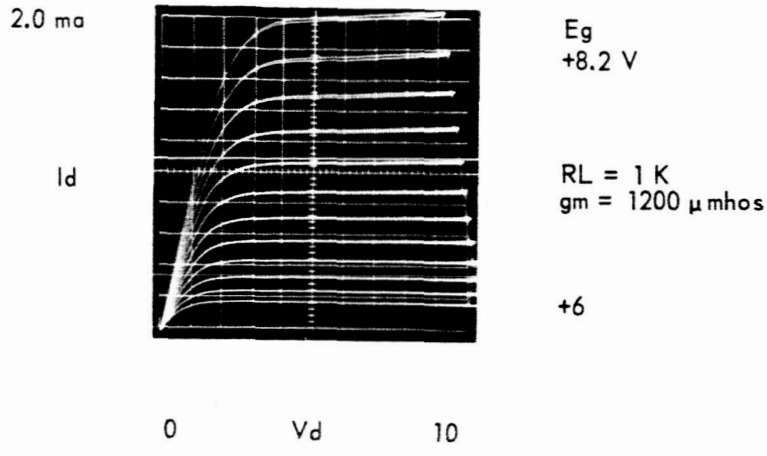


Figure 9. Characteristics of CdSe TFT

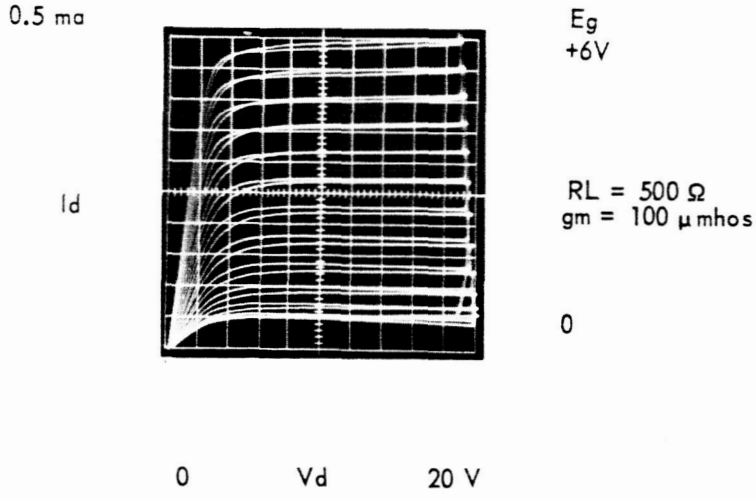


Figure 10. Characteristics of CdS TFT

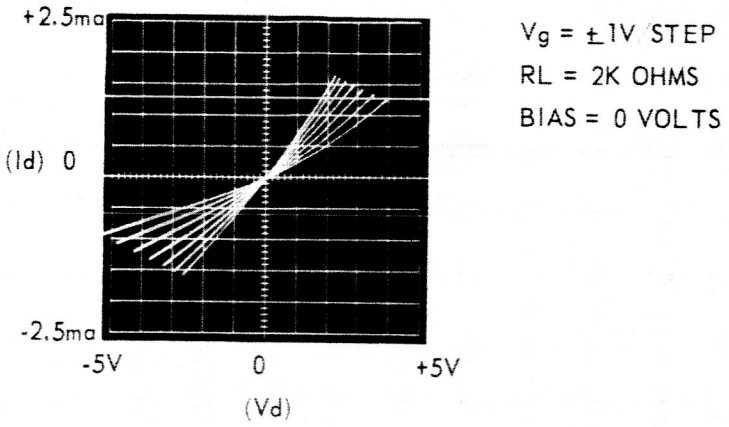


Figure 11. Characteristics of CdTe TFT

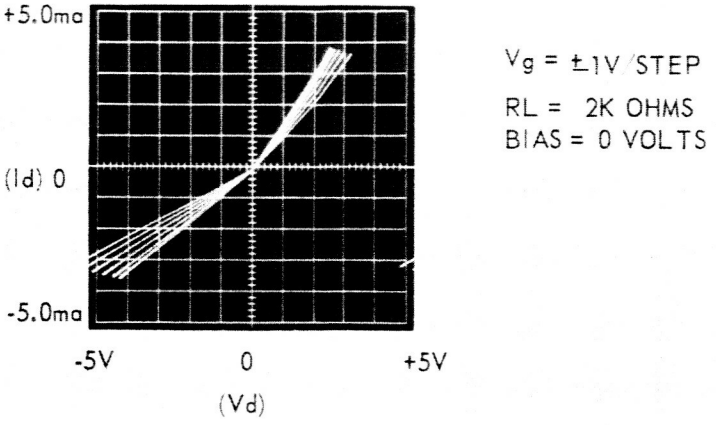
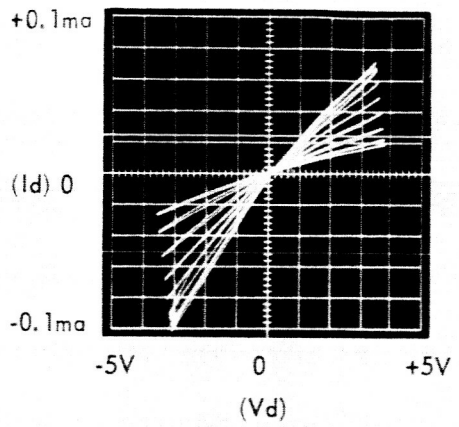
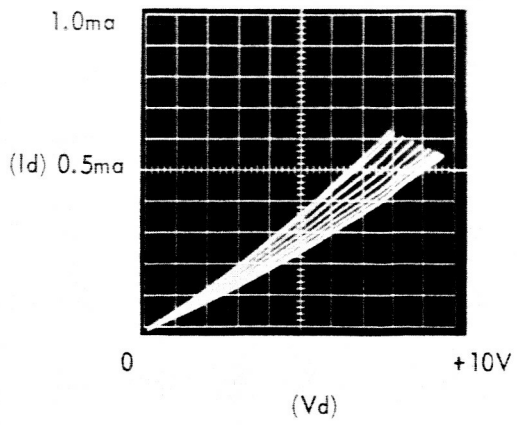


Figure 12. Characteristics of PbTe TFT



V_g = ± 2V STEP
RL = 2K OHMS
BIAS = 0 VOLTS

Figure 13. Characteristics of Ag_2Te_3 TFT



V_g = +2V STEP
RL = 10K OHMS
BIAS = +6 VOLTS
(BOTTOM STEP)

Figure 14. Characteristics of Bi_2Se_3 TFT

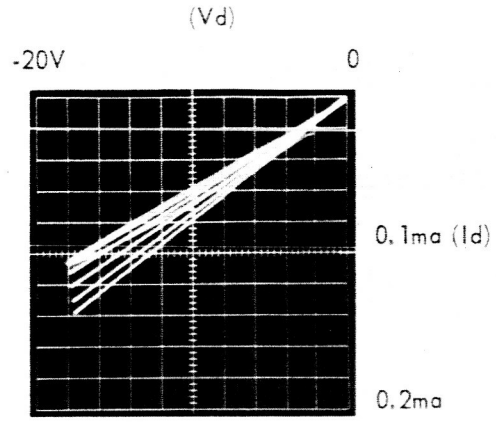


Figure 15. Characteristics of MnSe TFT

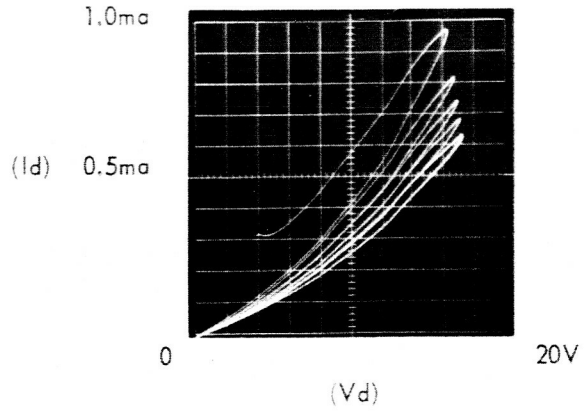


Figure 16. Characteristics of MnTe TFT

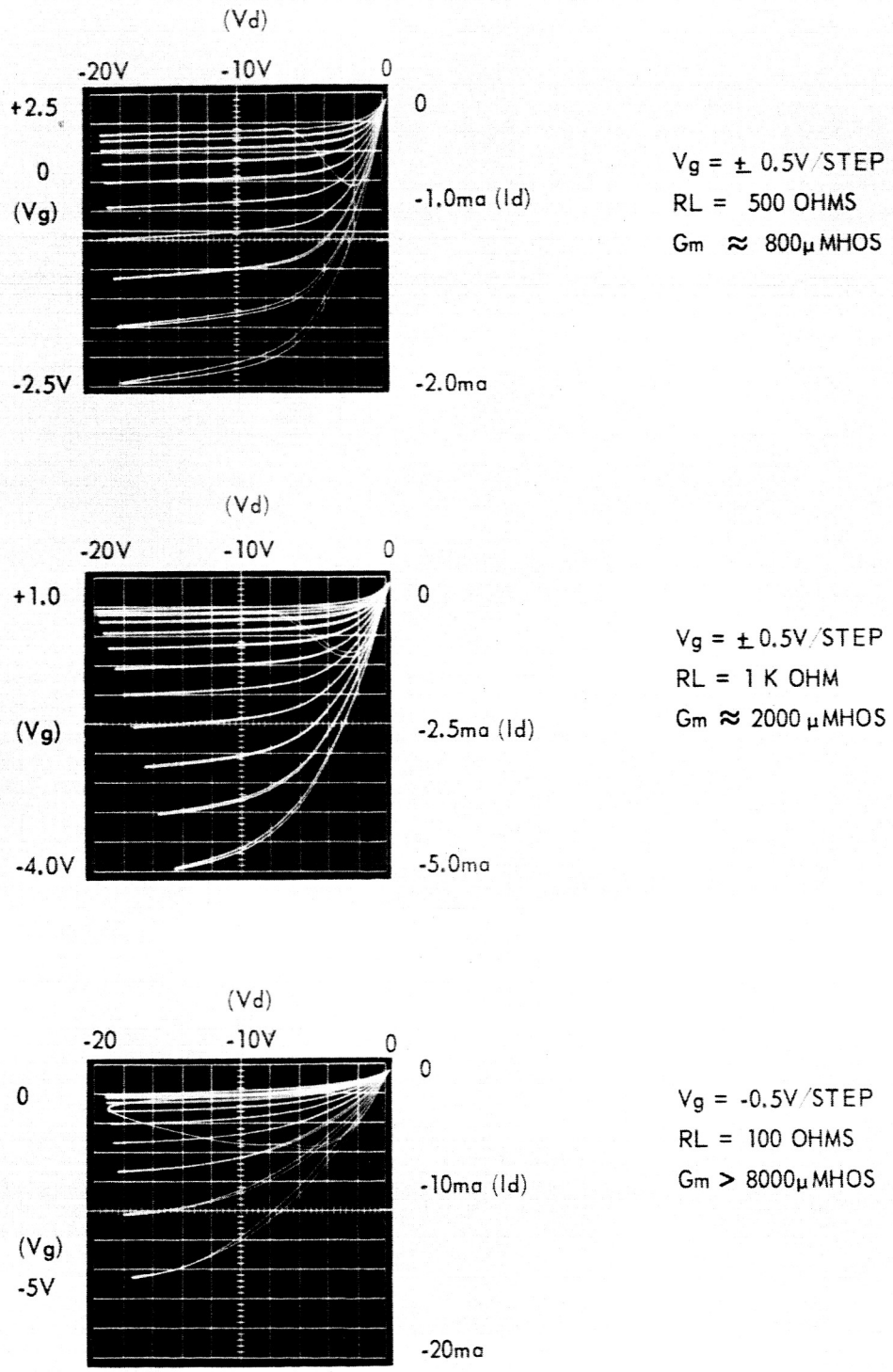
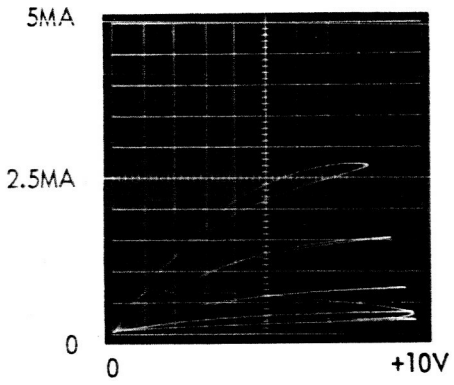
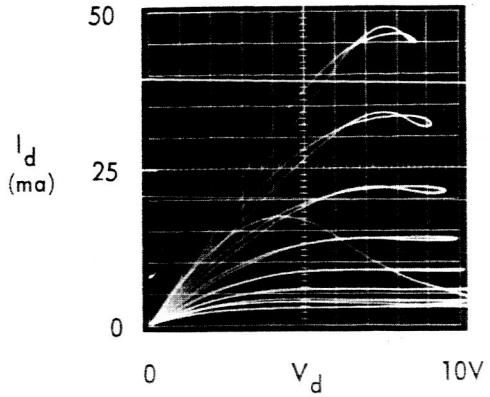


Figure 17. Characteristics of Te TFT's Operated at Different Bias Levels and Loads



V_g = 2V/STEP
R_L = 1K OHM
BIAS = -1.6V
n-TYPE MODULATION

Figure 18. Output Characteristics of CdTe Doped with Indium TFT



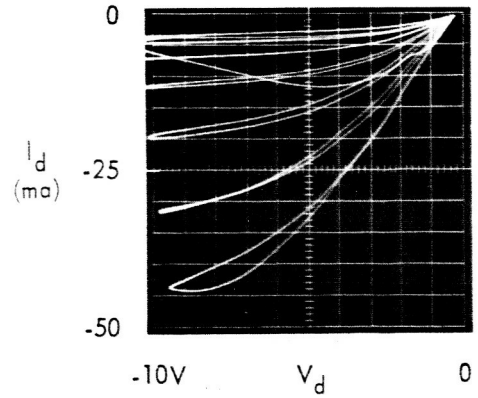
CdSe TFT

(a)

R_L = 20 Ω

$g_m \cong$ 25,000

V_G = +0.5 V/STEP



Te TFT

(b)

R_L = 20 Ω

$g_m \cong$ 25,000

V_G = −0.5 V/STEP

Figure 19. High Transconductance Thin-Film Triodes

2.4 TFT Structure and Overall Configuration

Figure 20 illustrates those basic configurations considered for the TFT. A discussion of alternate variations, advantages, and disadvantages are discussed in Quarterly Report No. 1.

Most of the devices formed in this program were of the "staggered" structure. Devices of the other structures were formed, but have thus far been found inferior in electrical parameters. Inferior characteristics of the coplanar and planar structures are believed to be primarily due to a dielectric-semiconductor interface reaction which appears to make the surface of n-type semiconductor films more highly conductive. In the case of p-type (Te) TFT's, the Te layer is not substantially affected. However, processing techniques have not as yet yielded Te TFT's of better quality or reproducibility when utilizing the latter two structures.

For low-frequency applications in the TFPCTS, a triode layout and configuration arrangement (shown in figure 21) was considered. In this arrangement 50 TFT's are deposited as 25 pairs with a common source electrode for each pair. These device pairs would be held to the lower frequency considerations (to 5 mc) due to gate electrode alignment.

In a single-row arrangement (shown in figure 22(a)) alignment (gate) is far less severe. High-frequency TFT's were attempted utilizing this arrangement. Figure 22(b) more clearly illustrates the electrode arrangement of the devices shown in figure 22(a).

2.4.1 Narrow Soruce-Drain Spacing

In the interest of high-frequency capability of the TFT, an effort to reduce carrier transit time between the source and drain electrodes was made by reducing the spacing.

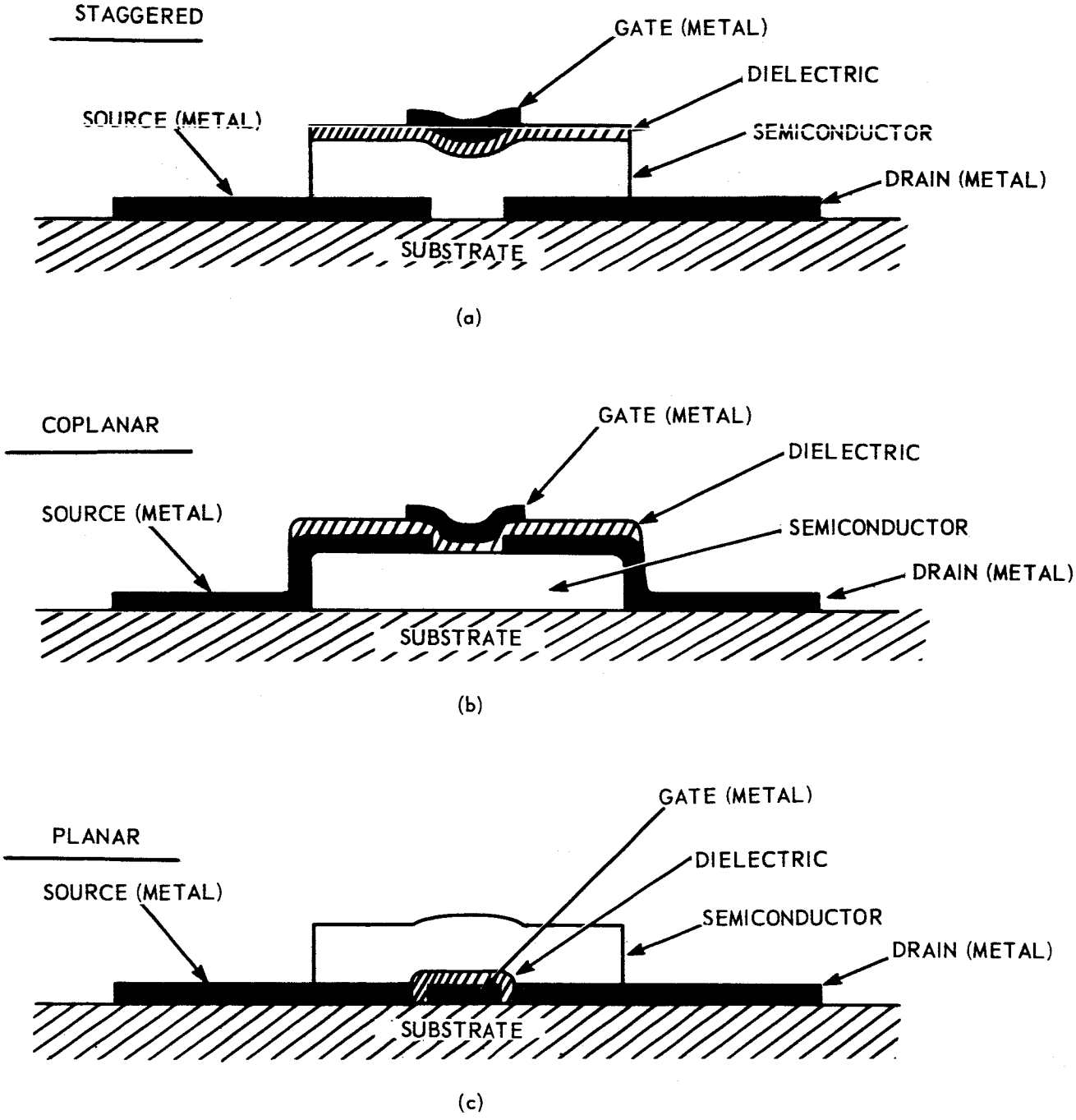


Figure 20. TFT Structures

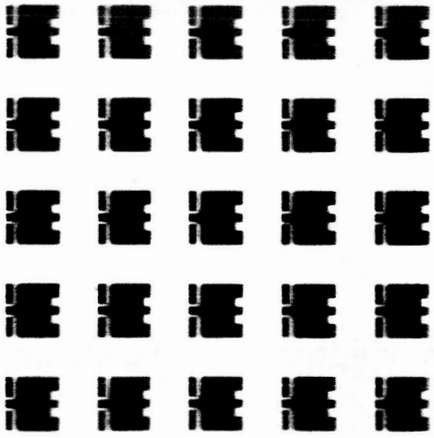
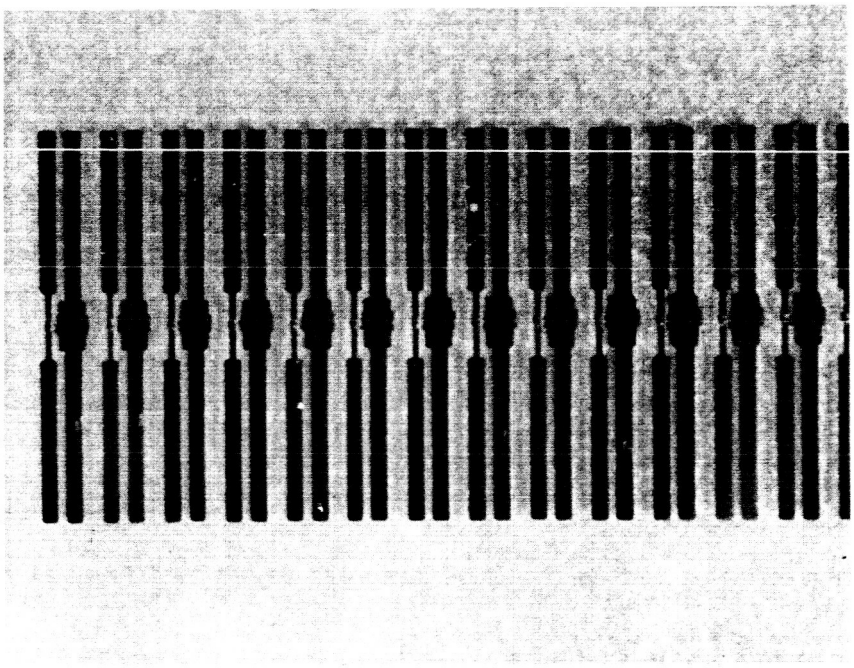
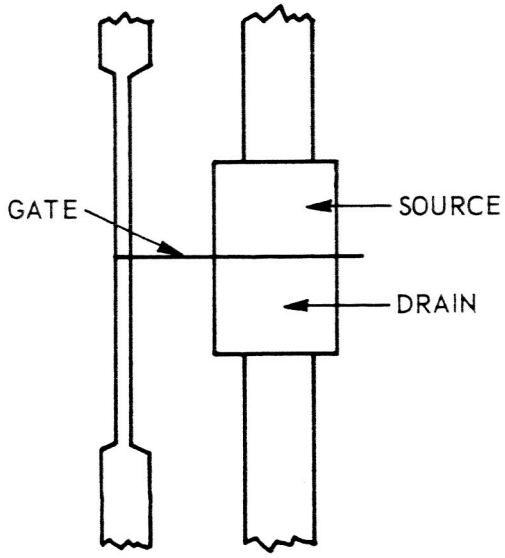


Figure 21. Common Source Arrangement of 25 TFT Pairs



(a)



(b)

Figure 22. High-Frequency TFT Configuration

During the course of this program, this space was narrowed to approximately 2.0 microns. A fine tungsten wire (Sigmund Cohn) attached to a basic electrochemically etched molybdenum mask was utilized. (Refer to Quarterly Report No. 3, page 11 for details.) For resolution, repeatability, and alignment accuracy, this technique was superior to the other techniques tested (etching, scribing, etc.). It would be advantageous, however, to have this requirement done with etching techniques, provided improved techniques can be found. Therefore, further studies of this method are to be made.

Figure 23 is a photomicrograph (42X) of a source-drain spacing of 2.5 microns. Due to the magnification, only a portion of the electrode separation is shown together with a small alignment pad (bottom of figure) which is deposited at the same time. (Refer to Quarterly Report No. 3, page 16.) The high yield (>95% for 2.5-micron spacing) of this deposition was very encouraging and implied that the technique was practical. Yield was determined on the basis of an open-circuit measurement (>1000 megohms) between the source and drain electrodes after their formation.

2.4.2 Formation of Narrow Gate Electrodes and Alignment to Source-Drain Spacing

Forming masks (chemically, electrochemically, or electroformed) of suitable resolution is limited to openings or land areas. At present, the state of the art is generally such that dimensions of etched lines or land areas are dependent on mask thickness. This limitation, at present, is that the minimum etched line width be equal to mask thickness. Down to 1.0-mil openings (25 microns), therefore, there is little problem. Openings smaller than 1.0 mil, however, cause the mask to become very

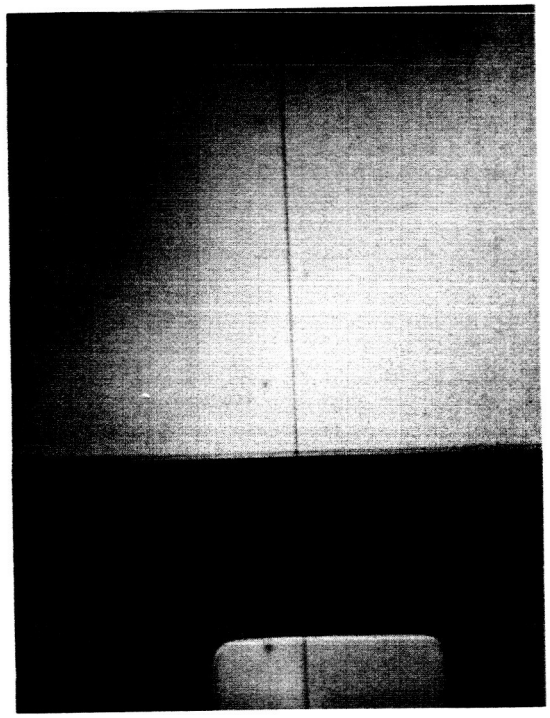


Figure 23. Source-Drain Electrode Evaporation (42X)

flimsy and hard to handle. Furthermore, scratches in the masking or mother material seriously imperil the resolution of fine etching or electroforming.

Another serious problem appears when masks are formed with openings of less than 0.5 mil (12 microns). This problem appears in the aluminum deposit for the gate electrode. Regardless of deposition techniques and good vacuum ($5x10^{-7}$ torr), aluminum deposits made through narrow mask openings take on an oxidized or nonconductive nature, depositing from a yellow (semiconducting) to black (nonconducting) layer. This is particularly true when thicker masks of relatively small openings are used. This is believed due to the pickup of loosely held oxygen atoms attached to the mask opening area by aluminum atoms passing (or bouncing) through.

After considerable effort at mask-making (electrochemically, chemically, and electroformed), a decision was made to utilize two 1.0-mil tungsten wires. These wires were used to define the gate electrode deposit (between them). The method of attaching these wires to a basic molybdenum mask is shown in Quarterly Report No. 3, page 17.

Aluminum deposits made between these wires was highly conductive down to 1.0 micron. It appeared that even narrower conductive aluminum deposits could be made. No real explanation can be made at this time as to why these deposits were conductive and those through solid masks were not. It is possible that the reason is the effect of a tapered opening and the relatively thin rounded edges limiting the outline of the deposit.

Figure 24 is a photomicrograph (240X) of a portion of a gate electrode formed by a deposit through an electrochemically etched molybdenum mask. The width of this deposit is approximately 2.0 mils. This mask is used on the low-frequency TFT's (pairs as shown in figure 21). Figure 25 is

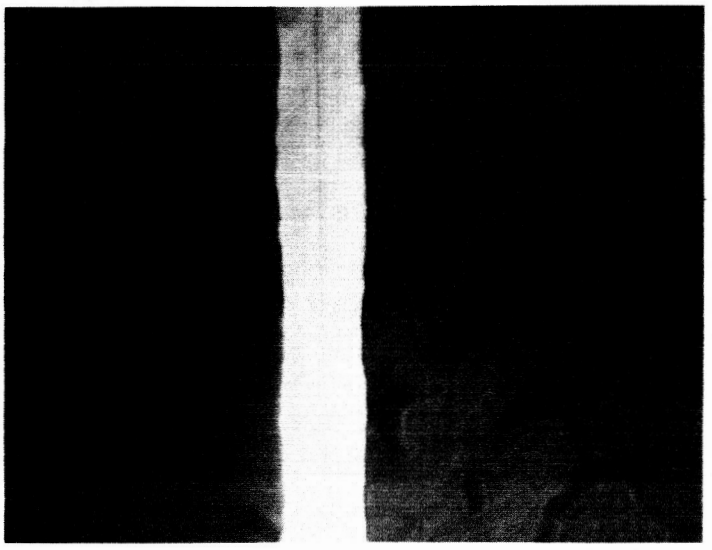


Figure 24. Gate Electrode Formed by Electrochemically Etched Molybdenum Mask (240X)

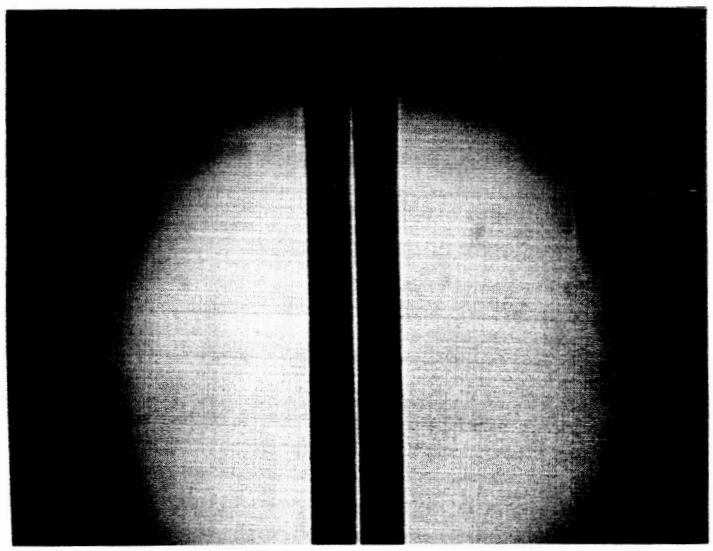


Figure 25. Gate Electrode Formed by Tungsten Wires (240X)

representative of the improvement obtained when utilizing tungsten wires to define the gate electrode. This latter photomicrograph (also 240X) clearly shows the outline of the two 1.0-mil tungsten wires (dark stripes) that limit the width of the gate electrode (center light line) to less than 0.2 mil (5 microns).

Such improvement in depositing the gate electrode vastly reduced input capacity of TFT's by a factor of at least 5:1. TFT's of less than 10 micro-microfarad input capacity are now being formed.

This technique of gate masking also opened several other avenues of investigation for improvement of the TFT:

a. It is now possible to deposit gate electrodes narrower than the source-drain spacing. This will allow adjustment in location of the gate to a portion of the channel. It may be possible, therefore, to reduce feedback (Miller) capacities to a minimum.

b. This technique may also allow further investigation of the in-line planar-type TFT structure. Figure 26 is a photomicrograph (240X) that shows a nichrome source- drain electrode deposition and an aluminum gate electrode deposit that has been deposited within the gap. In this arrangement a 5-micron gate has been deposited in a 7.5-micron source-drain spacing.

By oxidation of the aluminum gate electrode (by heat or anodizing), the planar-type structure is completed with the semiconductor deposit.

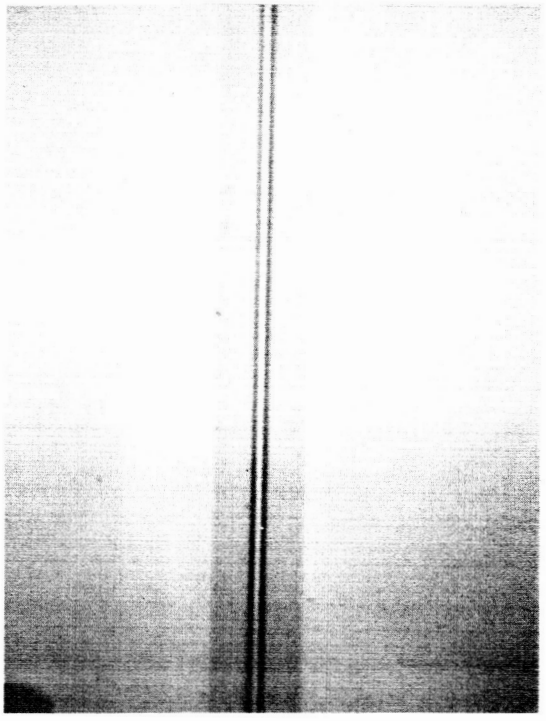


Figure 26. Deposited Electrodes for Planar TFT Structure

2.5 High-Frequency Measurements of TFT's

During this quarter TFT's were formed with input (gate) capacities of less than 10 micro-microfarads. These devices (Te or CdSe) often exhibited a transconductance of more than 5000 micro-mhos. From the approximate gain bandwidth product equation ($GBW = \frac{gm}{2\pi C}$), it would be expected that a bandwidth of greater than 80 mc might be achieved.

Measurements of these devices yielded GBW to 33 mc. A tellurium TFT was tested under resonant circuit conditions. It exhibited a voltage gain of 2 at 93 mc, but deteriorated before the ultimate frequency of oscillation was achieved. Such deterioration (usually loss of pinch-off) was noted often in high-frequency tests and contributed to a further device investigation of this problem.

Three possibilities may contribute to the device deterioration in high-frequency tests. These are discussed in the following paragraphs.

2.5.1 Test Procedure and Setup

Often in attempting to obtain maximum capability of the device, certain electrode voltages were exceeded. This was done intentionally to acquire knowledge of the device's durability and maximum capability.

It was also found that devices were often damaged while under test if leads of such instruments as voltmeters, etc., were attached or detached. This damage is believed due to inductive or static charges which exceeded the dielectric or semiconductor breakdown strength.

2.5.2 Electrode Diffusion

In attempting to determine high-frequency capability, the source-drain electrode spacing has been reduced to 2 microns. This action was

expected to reduce carrier transit time and to increase transconductance by a like ratio. However, below a 5-micron spacing of the source-drain electrodes, little improvement in transconductance has been realized and another problem begins to appear.

This problem is poor field effect (transconductance and pinch-off). Characteristics of the device imply a heavy doping of the semiconducting channel. This doping could only come from the source-drain electrodes themselves.

It is believed that nichrome made an excellent ohmic contact to many of the semiconductor films (in spite of its work function in regard to the CdSe conductivity type), because the metal semiconductor barrier was reduced by diffusion of the two materials.

The nichrome diffuses into the semiconductor layer, probably forming a portion of the channel that does not exhibit field effect and has high carrier concentration. This, in turn, limits the overall field effect of the channel. If the source-drain spacing is much more narrow than anticipated (i.e., smaller than the wire mask diameter) such that actual submicron spacing is achieved, a further diffusion of a few thousand angstroms by the electrodes into the channel may, in fact, short the channel with a highly conductive composite that exhibits very little field effect.

Figure 27 illustrates the possibility which may exist in narrow source-drain electrode spacings. The dashed line circle represents the wire mask used in the source-drain electrode formation. Due to vapor collision in the nichrome deposition, the rounded edges of the wire allows the leading

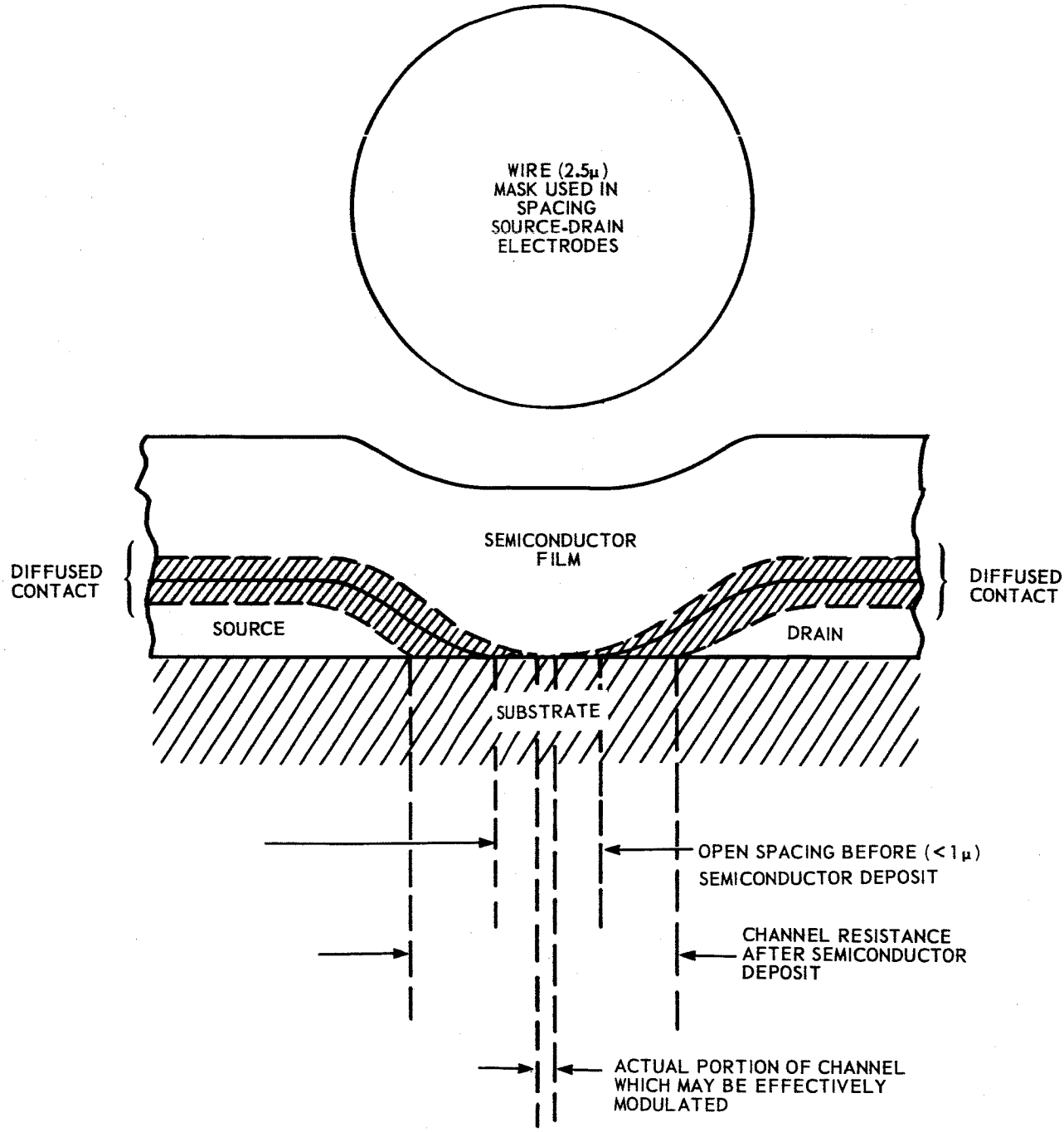


Figure 27. Electrode Diffusion in TFT Formation

edges of the nichrome to be somewhat closer than the wire diameter (i.e., possibly less than 1.0 micron).

The deposition of the semiconductor causes possible reaction with the nichrome, which may extend several thousand angstroms into the semiconductor as shown. The reacted or diffused mixture of semiconductor and nichrome exhibits no field effect, but it does have a resistive nature that tends to swamp the remaining portion of the channel which is non-contaminated and effectively modulated.

There is little doubt that the foregoing is happening, and an effort will be made to reduce the causes. This effort will include attempts to alter the deposition parameters to reduce the tapered edges of the electrodes as shown (better vacuum, greater evaporation distance, thinner source drain electrodes), and possibly to use other metals for the electrodes involved which react less with the semiconductor layer (i.e., gold, indium, etc.).

2.5.3 Dielectric Breakdown

As mentioned, many devices appeared to deteriorate because of dielectric failure. An effort to reduce this problem by depositing thicker SiO layers and alternate methods of deposition to improve the dielectric strength were undertaken. This effort appears to have succeeded in the low-frequency devices (i.e., greater gate and drain voltages -- to 20 volts -- could be used). It may be possible that high-frequency devices utilizing such a dielectric may withstand high-frequency tests at a reduced maximum rating of 10 volts.

3. METAL BASE TRANSISTOR AND DIODES

The ability to fabricate Au-ZnSe/CdSe junctions suitable for the collector and emitter sections of a thin-film metal base transistor was reported in the quarterly reports. A major problem that contributed to the delay in the investigation of complete transistor structures was the difference in the properties of the starting semiconductor materials. Materials from different suppliers, or batches of material from the same supplier, exhibited marked differences in their properties, resulting in widely varying junction properties.

The main effort during the past quarter was to fabricate complete metal base transistor structures. The CdSe and ZnSe material supplied by Koch-Light Laboratories was used almost exclusively for the collector junctions. Emitter junctions were formed with either Koch-Light or Harshaw CdSe and Koch-Light ZnSe. Although the properties of the collector and emitter junctions were difficult to optimize, due to the differences exhibited by the starting materials, the completed structures exhibited transistor action and showed power gain greater than unity when the base layer was made less than 500 A thick.

3.1 Fabrication Techniques for Au-CdSe/ZnSe-Au-ZnSe/CdSe-Au Metal Base Transistors

The collector structure, consisting of a mixed CdSe-ZnSe system between two gold electrodes, is first deposited on a 20-mil glass (Corning Code 0211) substrate. The first gold electrode is deposited to a thickness of 800 A to 1000 A at a rate of about 100 A/second and a substrate temperature of about 200°C. The semiconductor mixture is then deposited at a substrate temperature that ranges from 200° to 250°C to a thickness of about 10,000 A

at the rate of about 1,700 A/second. The CdSe and ZnSe components are mixed together and deposited from a single graphite crucible. The crucible is gradually heated. This allows the CdSe component to be deposited first, followed by a coevaporation of CdSe and ZnSe, and finally resulting in a ZnSe-enriched component. The film is thus graded and a blocking gold contact is evaporated, at a substrate temperature of about 50°C, onto the ZnSe-enriched surface. This gold contact, which forms the metallic base layer of the transistor, is deposited at a rate of about 100 A/second to the desired base thickness. In the structures fabricated, this thickness ranged from approximately 100 A to 800 A.

The emitter structure is then deposited on top of the collector structure. Since the emitter semiconductor must form its blocking contact at the emitter-base interface, it is necessary to form the emitter semiconductor with its ZnSe-enriched region at the base contact. The single-crucible procedure, used in evaporating the collector semiconductor, cannot be used. Because of the difference in vapor pressure between the two semiconductors, this technique always forms a deposit with a CdSe-enriched bottom surface and a ZnSe-enriched top surface. The emitter semiconductor is therefore formed by depositing each component separately from two graphite crucibles. The crucibles are heated so that a ZnSe-enriched region is formed at the base interface and a CdSe-enriched region is formed at the uppermost surface. The emitter semiconductor is deposited to a thickness of about 15,000 A at a rate of about 2,000 A/second. The temperature of the collector structure, which is the "substrate temperature" for the emitter semiconductor, is held to about 100°C. A gold

emitter electrode, about 1000 A thick, is then deposited onto the emitter semiconductor.

The entire structure and mask layout are shown in figure 28. The masks are made from 5-mil molybdenum. They are set up so that 4 devices can be fabricated per substrate and 16 devices fabricated per deposition. The active region of the transistor is 0.0625 square inch and is about equal to the diameter of the emitter electrode.

3.2 Characteristics of Au-CdSe/ZnSe-Au-ZnSe/CdSe-Au Metal Base Transistors

Figure 29 shows the characteristics of three different thin-film metal base transistors operating in the ground emitter configuration. These characteristics were displayed on a Tektronix 575 transistor curve tracer. The "prebias effect" seen at the origin of each curve is caused by base current flowing directly to the collector, which is forward-biased as the base voltage goes positive. As the collector voltage is increased positively, the collector is reverse-biased and the collector current from the base is forced into the emitter. When this occurs, transistor action begins. The hysteresis loops, exhibited markedly by transistor (c), are due mainly to the collector junction capacitance.

The calculated values of β (common emitter current gain) for each transistor are 0.0085, 0.02, and 0.25, respectively. The improvement from transistor (a) to transistor (b) is due mainly to the reduction in the collector barrier height. This reduces the reflection of carriers at the collector barrier. The vast improvement exhibited by transistor (c) is due both to a further reduction in the collector barrier height and to a reduction in the base layer thickness. This reduction in thickness improves the transmission of electrons through the base region and increases the collection probability.

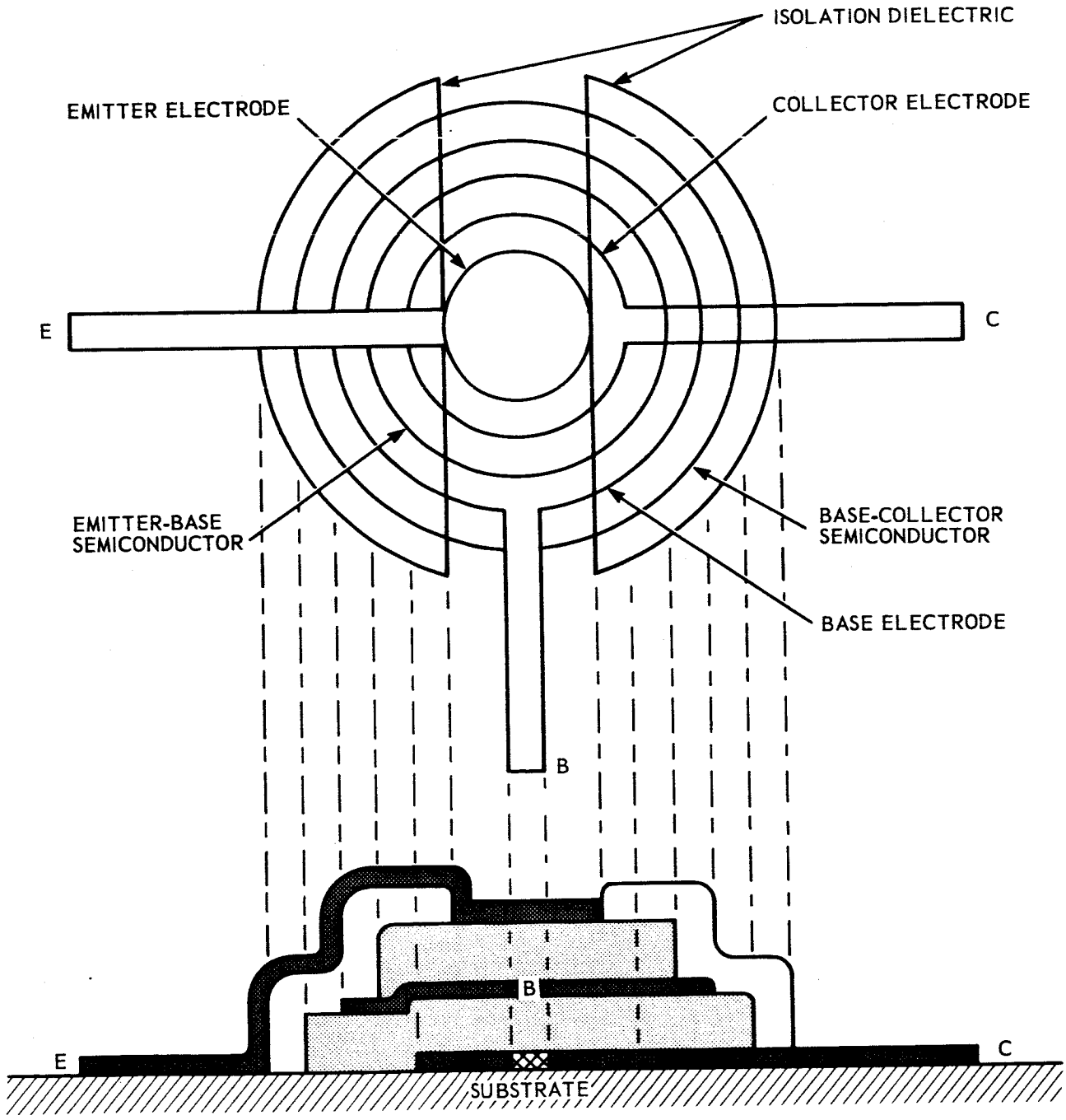
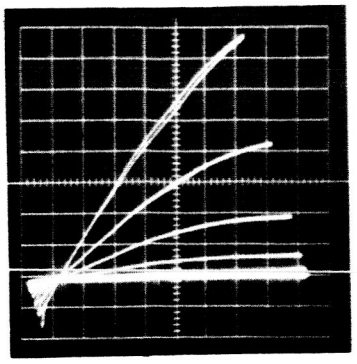
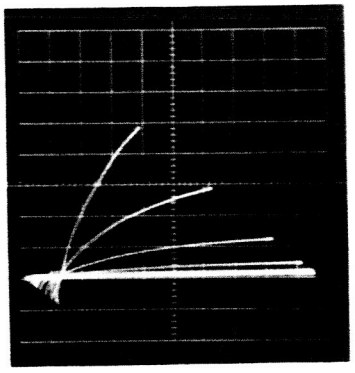


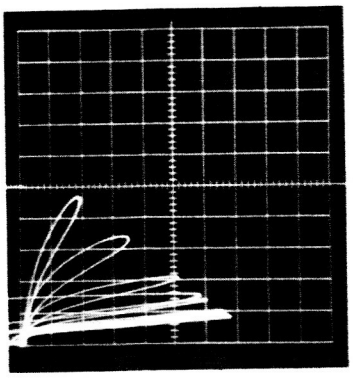
Figure 28. Mask Layout and Deposition of Metal Base Transistor



a) Au BASE THICKNESS ≈ 800Å



b) Au BASE THICKNESS ≈ 800Å



c) Au BASE THICKNESS ≈ 350Å

Figure 29. Characteristics of Three Different Thin-Film Metal Base Transistors (Grounded Emitter)

Transistor (b) exhibits a voltage gain of about 6 with a 10,000-ohm load resistor. This transistor exhibits no power gain. Transistor (c) exhibits a power gain of 2 at 120 cps with a 20,000-ohm load resistor. Further reduction in base thickness is required to achieve current gain. Assuming a reflection coefficient of 40% at the collector barrier, a gold base thickness of about 120 A is required for the transistor to exhibit current gain.

3.3 Phase A Summary

The work on the thin-film metal base transistor was initiated as an alternate approach to an ultrahigh-frequency amplifier. This type of device was judged to be worth investigating for two main reasons: (1) the device appeared to be especially attractive to construct by deposition techniques, because the semiconductor portions of the device could be polycrystalline in structure and because a very narrow thickness was required for the base region; and (2) the device has a predicted frequency capability of 100 gc. This high-frequency capability is made possible by the extremely small carrier transit time through the base region and by the small base resistance offered by the metal film.

To construct the transistor, suitable metal-semiconductor junctions had to be developed for eventual use as the emitter and collector sections. Melpar's approach toward the fabrication of a thin-film metal base transistor was, therefore, as follows:

a. To develop suitable collector and emitter metal-semiconductor junctions. These junctions were to be of an all-evaporated structure suitable for incorporation into thin-film integrated circuits.

b. To incorporate these junctions in a metal base transistor structure and to study device feasibility.

c. If device feasibility could be demonstrated, and if the amplifier characteristics were encouraging, the effort would be directed toward high-frequency operation and device development for possible application in the TFPCTS.

3.3.1 Metal-Semiconductor Junctions

Thin-film junctions, suitable for both the emitter and collector sections of a metal base transistor, were fabricated by vacuum-depositing a graded CdSe-ZnSe film between two deposited gold electrodes. Gold was chosen as the electrode material since the mean free path of electrons in gold has been reported to be about 740 A for energies between 0.8 and 1.1 ev.

The semiconductor film was deposited in a manner wherein the ZnSe concentration was greatest at the boundary where the junction was desired. The barrier height of the junction could be varied from approximately 0.2 to 2.0 ev by changing the relative concentrations of the compounds. The ability to control the barrier height made these junctions particularly suitable for metal base transistor facrication, since the collection efficiency is dependent on the relative barrier heights of the emitter and collector.

An analysis of these junctions indicated the presence of a Schottky-type barrier at the blocking contact. The barrier heights and doping profiles were determined by differential capacitance methods.

Switching measurements showed the insignificance of charge storage and minority carrier redistribution as limitations to high-frequency response. This confirmed the unipolar nature of the conduction mechanism.

Shelf life tests on unencapsulated junctions showed no failures after 5000 hours. Continuous operational tests on five junctions showed no failures after 300 hours. Storage in vacuum for 1 hour at 160°C caused no permanent damage or changes. The ability of the junctions to withstand this temperature in vacuum made them compatible with the anticipated fabrication temperatures of the "reverse" junction.

3.3.2 Varactor Applications of Au-CdSe/ZnSe-Au Junctions

The theory of varactor operation was analyzed, and some discrepancy was found between the theoretical predictions and the experimental results. The discrepancy was attributed mainly to the nonuniformity of the effective space-charge density in the depletion region.

Preliminary varactor measurements were performed on units with a 7500-A-thick semiconductor and a 5.81×10^{-2} cm^2 area. Measurements were made with a capacitance bridge using a $\frac{1}{2}$-volt, 100-kc signal. Typical values for capacitance ratio, obtained over a bias range of 3.5 volts, were from 1.1 to 1.2. The relatively large area restricted the zero bias cut-off frequency to about 1.5 mc. A reduction in junction area would have been necessary to increase the cut-off frequency by several orders of magnitude.

3.3.3 Metal Base Transistors

An analysis of the high-frequency response of a metal base transistor was outlined, and the important geometrical and physical considerations were discussed in the First Quarterly Report. The necessity for a theoretical understanding of the device operation prior to device fabrication is obvious.

Metal base transistor structures, exhibiting power gains greater than unity, were fabricated by coupling two Au-CdSe/ZnSe junctions back-to-back. Their characteristics are shown in figure 29 and discussed in section 3.2.

Although the work did not progress far enough to realize a practical amplifier, the fabrication of amplifying thin-film metal base transistor structures was considered a significant achievement.

3.3.4 Material Evaluation

One of the main problems in the reproduction of Au-CdSe/ZnSe junctions was the difference in junction properties arising from differences in the properties of the starting semiconductor materials. Table 1 shows the characteristics of junctions formed from ZnSe obtained from different suppliers. CdSe from Koch-Light Laboratories was used in all cases. The spectrographic analysis report on these materials is given in table 2.

The relationship between the properties of the starting semiconductor material and the properties of the deposited junction is not understood. Such an investigation would require more research effort. To reproduce devices, such a study would be necessary to specify the raw material properties of the semiconductor manufacturers.

3.4 Phase A Conclusions

The conclusions drawn from a year's research effort on thin-film metal base transistors include:

a. Excellent thin-film diodes can be fabricated by vacuum deposition techniques. These "hot electron" diodes can be fabricated by using a CdSe/ZnSe semiconductor system in contact with a gold blocking electrode. Their varactor properties merit further investigations.

TABLE 1

CHARACTERISTICS OF JUNCTIONS FORMED FROM ZnSe FROM DIFFERENT SUPPLIERS*

ZnSe Supplier	Peak Inverse Voltage (volts)	Forward Breakdown Voltage (volts)	Rectification Ratio	Forward Resistance (ohms)	Leakage Current at -4 Volts (μa)
Penn Rare Metals, Inc.	8-10	0.3-0.8	10^4-10^5 at 1 volt	≤100	≤1
Koch-Light Laboratories, Inc.	8-10	0.2-0.6	10^4-10^5 at 1 volt	≤100	≤1
Metal Hydrides, Inc.	5-6	2-3	10^4 at 3 volts	≤500	≤1
Harshaw Chemical Co.	3-4.5	0.4-0.8	10^4 at 1 volt	≤500	≤2
Kern Chemical Corp. (luminescent grade)	6	0.3-0.8	10^4-10^5 at 1 volt	≤200	≤1
Eastman Kodak Co.	3-4	0.3-1.5	10^4 at 1 volt	≤500	≤3
Kawecki Chemical Co.	3-4	0.3-1.5	10^4 at 1 volt	≤500	≤3

* Junction area is 5.81×10^{-2} cm^2.

TABLE 2

SPECTROGRAPHIC ANALYSIS REPORT OF
MATERIALS FROM VARIOUS SUPPLIERS

Material	Supplier	Impurities	Faint Impurities (<< 0.001%)
ZnSe	Penn Rare Metals, Inc.	Ca (~0.001%) Pb (~0.01%) Mg (~0.001%)	Al Si Cu Sr Fe
ZnSe	Koch-Light Laboratories, Inc.	B (~0.001%)	Cu Mg Sr
ZnSe	Matal Hydrides, Inc.	Fe (~0.005%) B (~0.01%) Ca (~0.001%) Cu (< 0.001%)	Al Mn Cu Si Mg Sr Al Mn
ZnSe	Harshaw Chemical Co.		Al Mg Cu Si Fe Sr
ZnSe	Kern Chemical Corporation	Ca (~0.001%) Cu (~0.005%) Al (~0.005%)	Fe Si Sr
ZnSe	Eastman Kodak Co.		Al Si Cu Sr Fe Ti
ZnSe	Kawecki Chemical Co.	B (~0.001%) Pb (~0.001%)	Mg Si Sr
CdSe	Koch-Light Laboratories, Inc.		Cu Mg Zn

b. It is feasible to construct an amplifying thin-film metal base transistor by coupling two of the above-described diodes through a thin gold base layer. More effort is required to realize a practical amplifier.

c. To aid in the reproduction of the above devices, the influence of the starting semiconductor material properties on the deposited junctions must be further investigated.

4. HIGH-FREQUENCY SUBSTRATE INVESTIGATION

4.1 Substrate Evaluation

A detailed substrate evaluation program was conducted during the first quarter of this phase and reported in detail in the First Quarterly Report.

Substrates of drawn glass, ground glass, ceramic, and sapphire were evaluated for the following properties:

a. Surface topology.

b. Compatibility with film materials.

c. Resistivity.

d. Dielectric constant.

e. Thermal conductivity.

f. Hygroscopicity.

g. Thermal stability

4.2 Conclusions

In general, most substrates were satisfactory for use in the TFPCTS. The ac surface resistivity changed as a function of frequency (capacitively) for all substrates. (See figures 30 and 31.) The effective ac surface resistivity at 220 mc was found to be of the same order of magnitude for all the substrates.

The drawn glass substrates were smoother and less costlier than the ground glass substrates. Of the drawn glass substrates, Corning Code 7059 had the higher ac surface resistivity and the lower alkali content.

The tested substrates and resultant findings are tabulated in table 3.

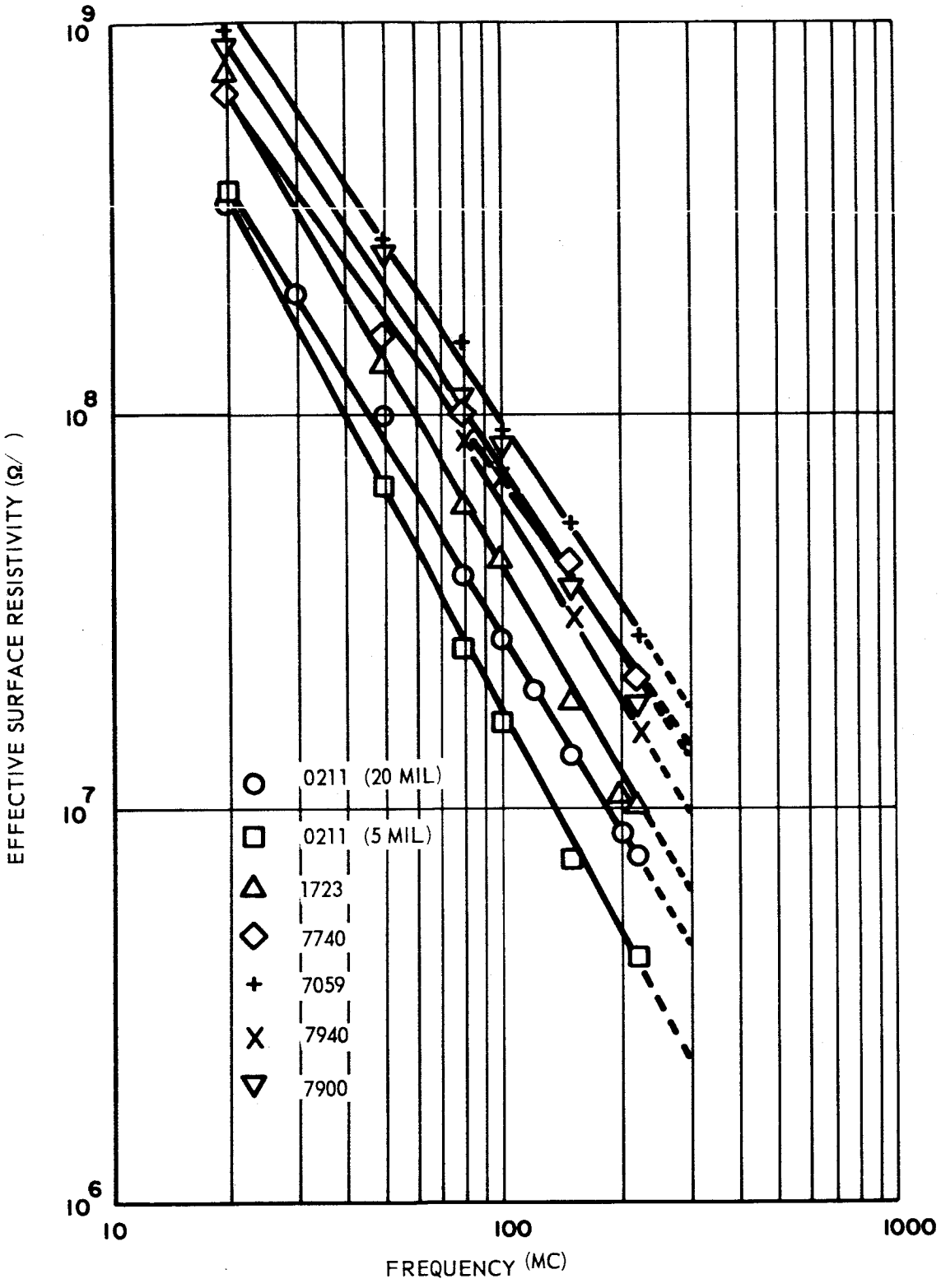


Figure 30. Frequency Dependence of Surface Resistivity of Several Glass Substrates

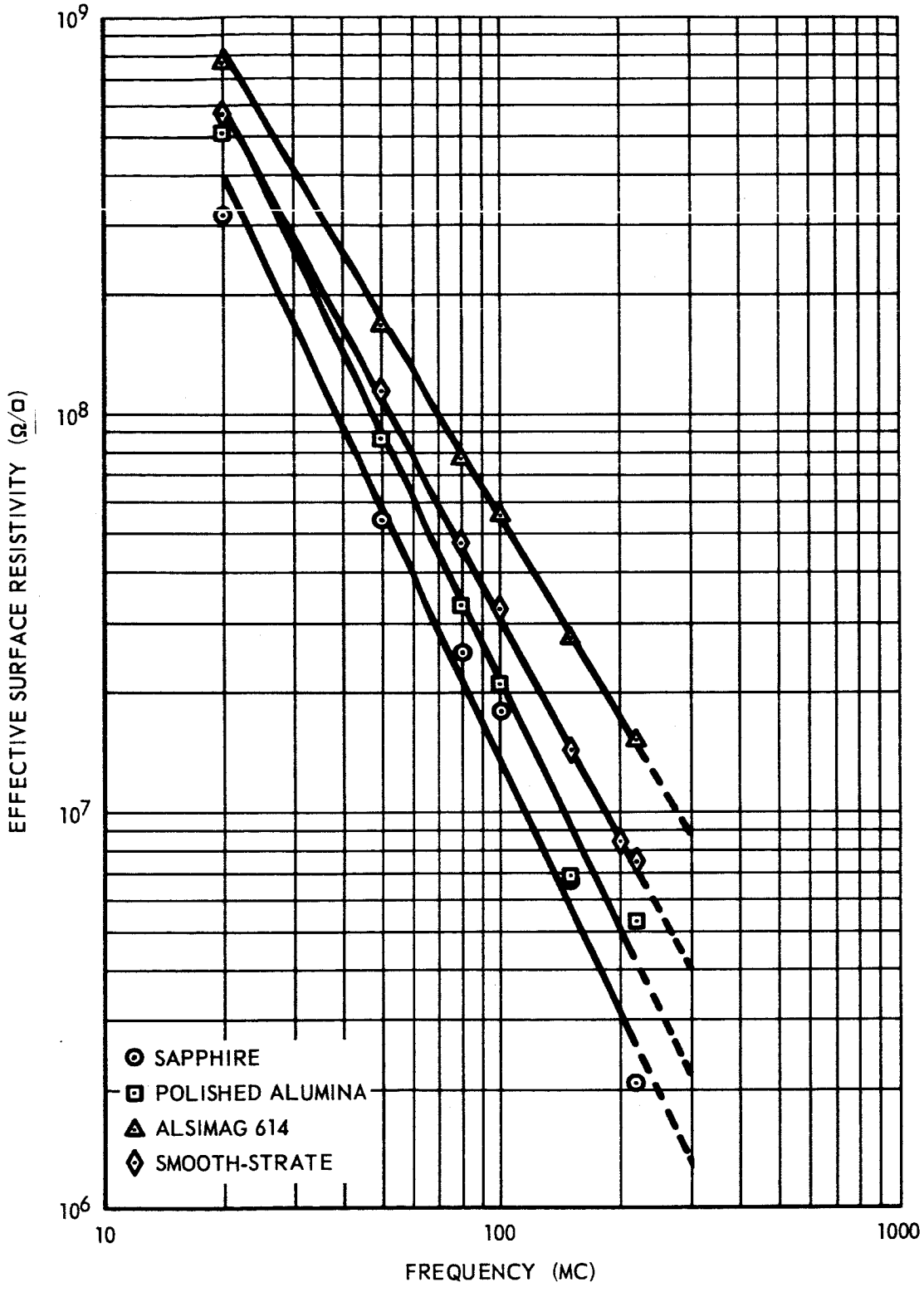


Figure 31. Frequency Dependence of Surface Resistivity of Several Basically Al_2O_3 Substrates

TABLE 3

CUMULATIVE SUBSTRATE DATA

Substrate Mfg and Code No.	Description	Surface Resistivity at 300 mc (Ω/sq)	Smoothness (-inch)	Flatness (inch/inch)	Expansivity $(^{o}C)^{-1}$	Softening Point (^{o}C)
Corning 0211 (Microsheet)	Alkali-zinc borosilicate glass	4.5×10^{6}	< 0.25	$\leq \pm 0.0004$	7.2×10^{-6}	720
Corning 1723 (Alkali-free)	Lime alumino-silicate glass	6.0×10^{6}	--	$\leq \pm 0.0002$	4.6×10^{-6}	912
Corning 7059 (Pyrex*) (Alkali-free)	Barium alumino-silicate glass	1.8×10^{7}	< 0.25	$\leq \pm 0.0004$	4.5×10^{-6}	872
Corning 7740 (Pyres*)	Alkali boro-silicate glass	1.45×10^{7}	--	$\leq \pm 0.0002$	3.25×10^{-6}	820
Corning 7900 (Vycor*)	96% silica boro-silicate glass	1.35×10^{7}	--	$\leq \pm 0.00005$	8.0×10^{-7}	1500
Corning 7940 (Alkali-free)	Fused silica	9.8×10^{6}	--	$\leq \pm 0.00055$	5.6×10^{-7}	1580
Insaco, Inc. (Linde) Sapphire	Single crystal Al_2O_3	1.3×10^{6}	< 5.0	$\leq \pm 0.00055$	8.7×10^{6}	--

TABLE 3 (Continued)

CUMULATIVE SUBSTRATE DATA

Substrate Mfg and Code No.	Description	Surface Resistivity at 300 mc (Ω/sq)	Smoothness (μ-inch)	Flatness (inch/inch)	Expansivity $(^{o}C)^{-1}$	Softening Point (°C)
AlSiMag* 753	Polished alumina ceramic	2.2×10^{6}	<20.0	$\leq \pm 0.00018$	6×10^{-6}	1650
Electro-ceramics (Smooth-Strate*)	Alkali-free, glazed alumina ceramic	4.0×10^{6}	< 0.5	$\leq \pm 0.00052$	6.65×10^{-6}	1816
AlSiMag* 614	Glazed alumina ceramic	8.7×10^{6}	Scratches prominent	± 0.0015	6.4×10^{-6}	1550

* Registered trademark.

5. DIELECTRIC INVESTIGATION

5.1 High-Frequency Capacitors

Thin-film capacitors were evaluated for high-frequency use during the second quarter of this phase. A detailed report is contained in the Second Quarterly Report.

Two different dielectric thin-film capacitors were compared with commercial high-frequency, silver-mica capacitors. The thin-film dielectric materials were SiO and a borosilicate mixture. The capacitors were operated up to a frequency of 400 mc.

5.2 Conclusions

The thin-film capacitors operated as satisfactorily as commercially available, high-frequency capacitors up to the limit of the testing -- 400 mc. The SiO dielectric performance was indistinguishable from the borosilicate, but the borosilicate dielectric material is preferable because of its higher dc resistance, its higher voltage breakdown strength, and its better temperature stability.

6. INDUCTORS

Research on the design and feasibility of thin-film inductors was done during the first three quarters of this phase. The fact that thin-film inductors are only two-dimensional and, of course, relatively thin compared to the skin depth at high frequencies necessitated detailed analysis of the resulting coils which were formed. Although the work was continuous, the results can conveniently be divided into sections coinciding with the first three quarters of this phase. The detailed reports are contained in the respective Quarterly Reports. The analyzed particulars are:

a. Inductance.

b. Self-resonance.

c. Q.

d. Resistance.

e. Skin depth.

6.1 First Quarter

Multiturn inductors were deposited and investigated. Flat, spiraling, square coils were used since this design provides the highest area efficiency and lowest intercoil capacitance with the simplest masking technique. Typical coils formed were:

L = 1.5 μh (inductance)

f_o = 110 mc (self-resonant frequency)

Q = 5 at 30 mc (inductor quality factor)

A = 0.36 square inch (area)

$L = 0.6\ \mu h$

$f_o = 160$ mc

$Q = 12$ at 30 mc

$A = 0.64$ square inch

The values of Q could be improved easily (thicker deposition of conductor) by a factor of 2.5. The self-resonant frequency figures are from the Third Quarterly Report.

6.2 Second Quarter

Inductors were formed in series aiding, and the inductance was increased by a factor of 4. For example, the 0.6-μh coil in section 6.1, when connected in series aiding with the same coil on the opposite side of the substrate, resulted in approximately four times the inductance.

$L = 2.7\ \mu h$

$f_o = 57$ mc

$Q = 8$ at 30 mc

The Q value could be easily increased 2.5 times by depositing a thicker film. Although the L is increased more than four times the value of a single coil, the Q remained the same as for a single coil. The self-resonant frequency figure is from the Third Quarterly Report.

6.3 Third Quarter

Single-turn inductors were formed for use at high frequencies. The self-resonant frequencies of these coils were well beyond 300 mc. Typical coils formed were:

$L = 0.04$ μh

$f_o = 1345$ mc (theoretical)

$Q = 50$ at 200 mc

$D = 0.4$ inch (outer diameter)

$L = 0.04$ μh

$f_o = 690$ mc

$Q = 80$ at 200 mc

$D = 0.8$ inch

Detailed evaluation of the effect of resistance and inductance was performed. Also, the effects of shielding were investigated and found to be only slightly degrading. Accurate values of the self-resonant frequency of the inductors formed in the first two quarters were determined by using a different piece of test equipment.

6.4 Conclusions

On 1-inch substrates, coils have been formed to achieve different inductances. The largest inductance was obtained with series aiding multi-turn inductors on opposite sides of the substrate. In this manner, inductances up to 3 microhenries were achieved with a Q of 8 at 30 mc and a self-resonant frequency of 54 mc as reported in the Second Quarterly Report. On one side of a substrate, 1.5 microhenries with a potential Q of 15 at 30 mc and a self-resonant frequency of 110 mc can be deposited in 0.36 square inch, as reported in the First Quarterly Report. Small-value inductors of 0.04 microhenry with a Q of 80 at 200 mc for use at high frequencies were reported in the Third Quarterly Report.

These inductors were completely formed by vacuum deposition through masks to make them compatible with monotronic circuits. The eventual circuit designs will determine whether they will be required in the TFPCTS.

7. THIN-FILM TRANSFORMERS

As reported in the Second Quarterly Report, the inductors were formed on both sides of a substrate, connected in series aiding, and resulted in four times the inductance obtainable with a single coil. This coupling looked promising for low-power transformer signal coupling.

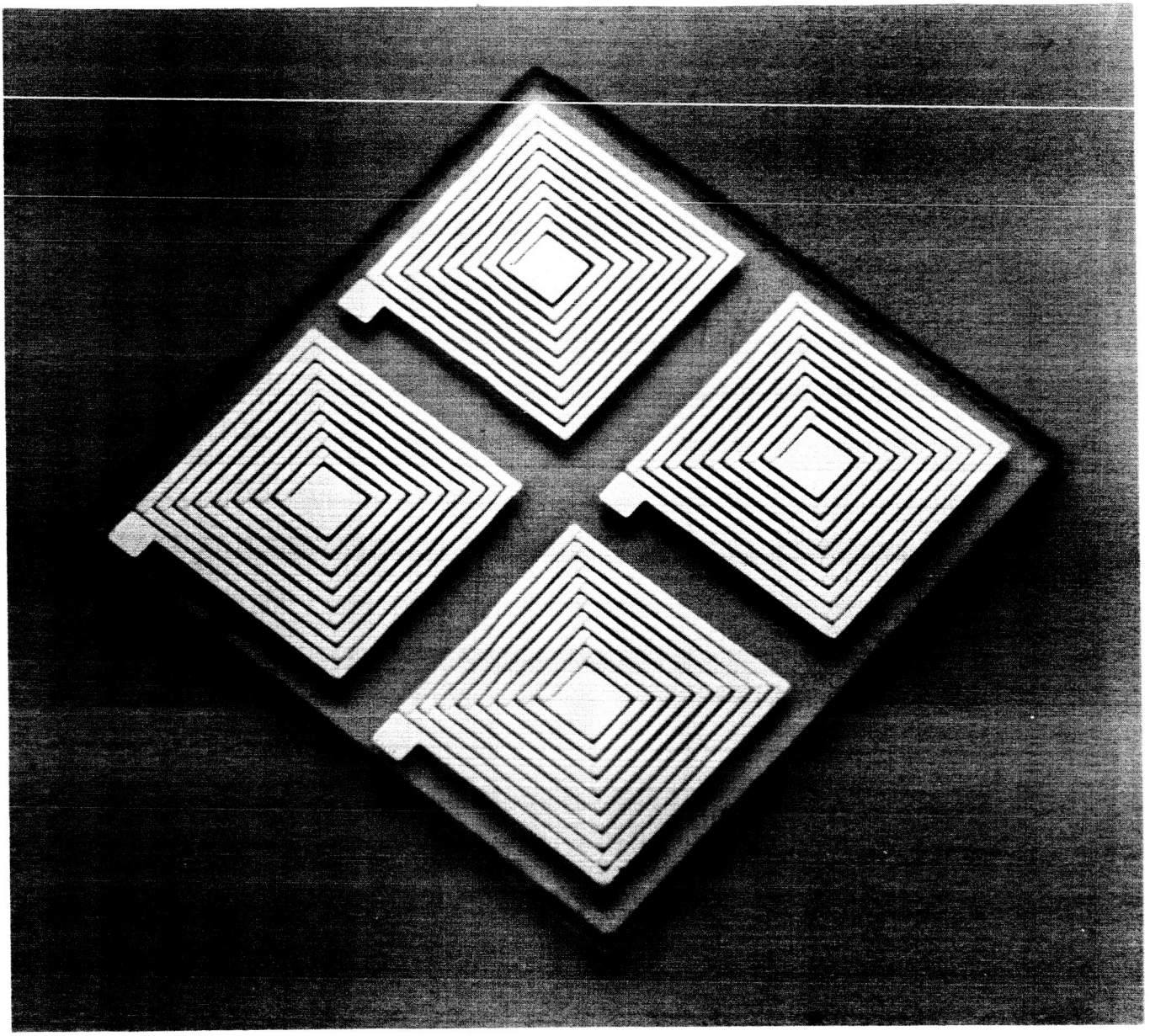
7.1 Transformer Theory

Successful transformer coupling of signals through glass substrates using thin-film coils was achieved during this last quarter. However, these transformers are very different from "ideal" transformers. For a transformer to approach an ideal transformer, it must have close coupling of the coils and the coil reactance must be high in comparison with the load impedance. If the coupling factor approaches unity, and if the coil reactance is much greater than the load reactance, the transformed impedance from the secondary to the primary is proportional to the coil turns ratio squared. Thus, there is no phase shift added by the transformer.

However, none of these items hold true for the thin-film transformers which were fabricated. The coupling coefficient through the glass was much less than 1. The reactance of the coils was approximately the same order of magnitude as the load, which was 50 ohms. The high-frequency oscilloscope (Tektronix 661) and the Hewlett-Packard VHF Signal Generator 608D were used.

7.2 Transformer Characteristics

The transformers reported herein were coils deposited on both sides of a substrate, with the coupling occurring through 20-mil-thick glass substrates (Corning Code 0211). Attempts to obtain coupling between coils side by side on the same substrate (figure 32) were unsuccessful.



Outer diameter = 0.4 inches
Conductor width = 0.010 inches (10 mils)
Spacing between conductors = 0.010 inches (10 mils)
Inductance = 0.5 microhenries
Q at 30 megacycles = 10

Figure 32. Thin-Film Inductors (Completely Vacuum Deposited)

Transformer T1, which has its coils described in table 4, showed transformer characteristics of almost 180° phase shift with an input to output voltage ratio of 3:2.1. The phase shift and voltage ratio changed as a function of frequency. These changes are tabulated in table 5 and shown graphically in figure 33. At 10 mc, the transformer operated satisfactorily; but as the frequency increased, the phase shift increased until at 212.5 mc the resulting effect was almost a pure capacitor. With increasing frequency, the capacitance between the coils with the substrate for a dielectric becomes more effective as a shunt path, as shown by the gradual phase shift from 180° out of phase to in phase. The decrease in the voltage ratio with frequency also shows the effect of shunting capacitance until the capacitance reactance is the dominating factor beyond 150 mc.

Transformer T2 has the same configuration as T1, except that the conductors are wider (table 4). The Q is lower because the conductor thickness was less than the coils on transformer T1. Transformer T2 (table 5 and figure 34) behaved very similarly to T1. The Q value did not seem to have any effect on the transformer operation.

Transformer T3 (figure 35) is also the same configuration as T1 and T2, except that it has wider conductors (table 4.) The reactance of the three coils was measured on the Boonton Radio RX Meter (250A), and the values are shown in table 4. The negative sign before the capacitance shows that the coils were all still behaving as inductors at 250 mc. They had not yet reached their self-resonant frequency when the capacitor between the coils through the glass substrates swamped out the transformers.

TABLE 4

INDUCTOR VALUES

Transformer	Conductor Width (mils)	Space (mils)	Outer Diameter (mils)	Inner Diameter (mils)
T1	15	35	0.8	0
T2	25	25	0.8	0
T3	35	15	0.8	0

Transformer	Actual L(μh)	Q (30 mc)	X_L (Ω) 10 mc	100 mc
T1	0.78	18	49	490
T2	0.79	7	49	490

Transformer	f(mc)	Resonating C. (pF)
T1	250	-2.8
T2	250	-3.8
T3	250	-4.6

1. Corning code 0211 substrates (1 inch square and 20 mils thick).
2. All values measured at 30 mc.
3. This table is reproduced from the Second Quarterly Report.

TABLE 5

PHASE SHIFT AND VOLTAGE RATIO CHANGES

Transformer	Frequency (mc)	Voltage Ratio (input/output)	Phase Shift (degrees)	Figure No.
T1	10	0.70	5	33 (a)
	50	0.37	45	(b)
	100	0.37	63	(c)
	150	0.40	83	(d)
	200	0.83	135	(e)
	212.5	0.80	180	(f)
T2	10	0.6	5	34 (a)
	50	0.43	45	(b)
	100	0.43	63	(c)
	150	0.47	83	(d)
	200	0.77	135	(e)
	222.5	0.73	180	(f)
T3	10	0.80	5	35 (a)
	50	0.53	45	(b)
	100	0.50	63	(c)
	150	0.53	83	(d)
	200	0.93	135	(e)
	223.5	0.87	180	(f)
T4	10	0.80	5	36 (a)
	50	0.47	45	(b)
	100	0.40	63	(c)
	150	0.43	83	(d)
	200	0.53	105	(e)
	249.6	0.97	180	(f)

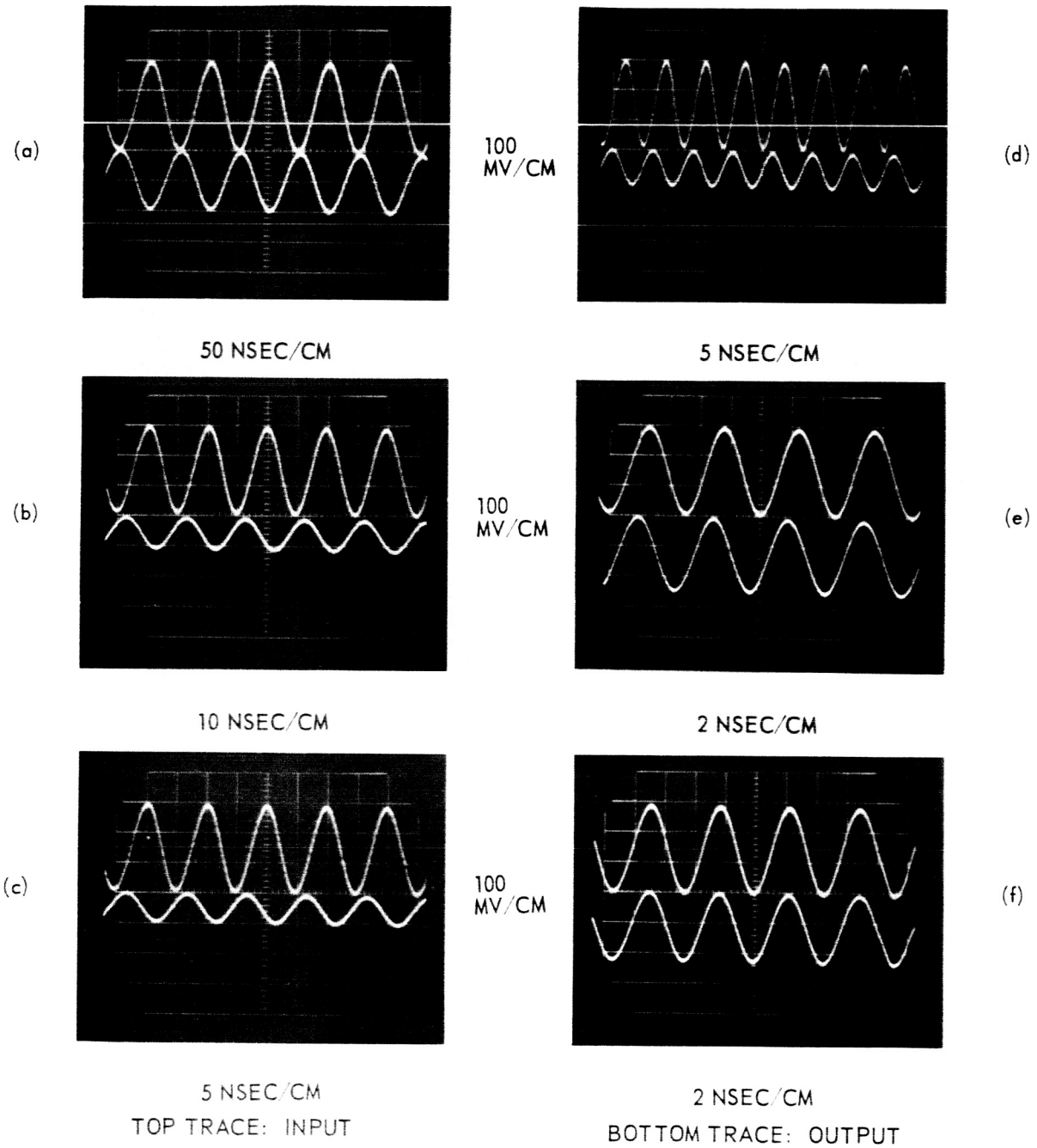


Figure 33. Transformer T1

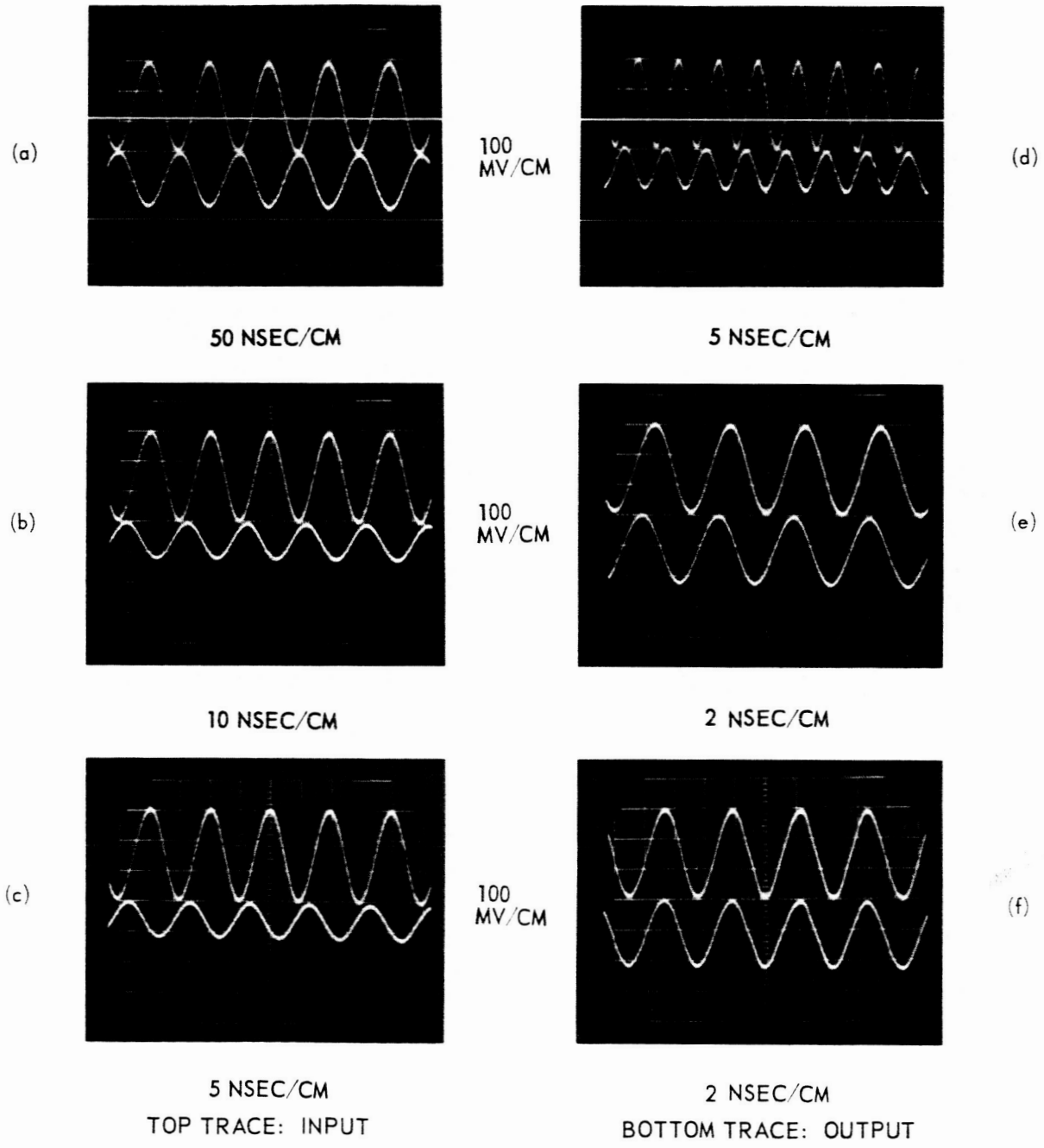


Figure 34. Transformer T2

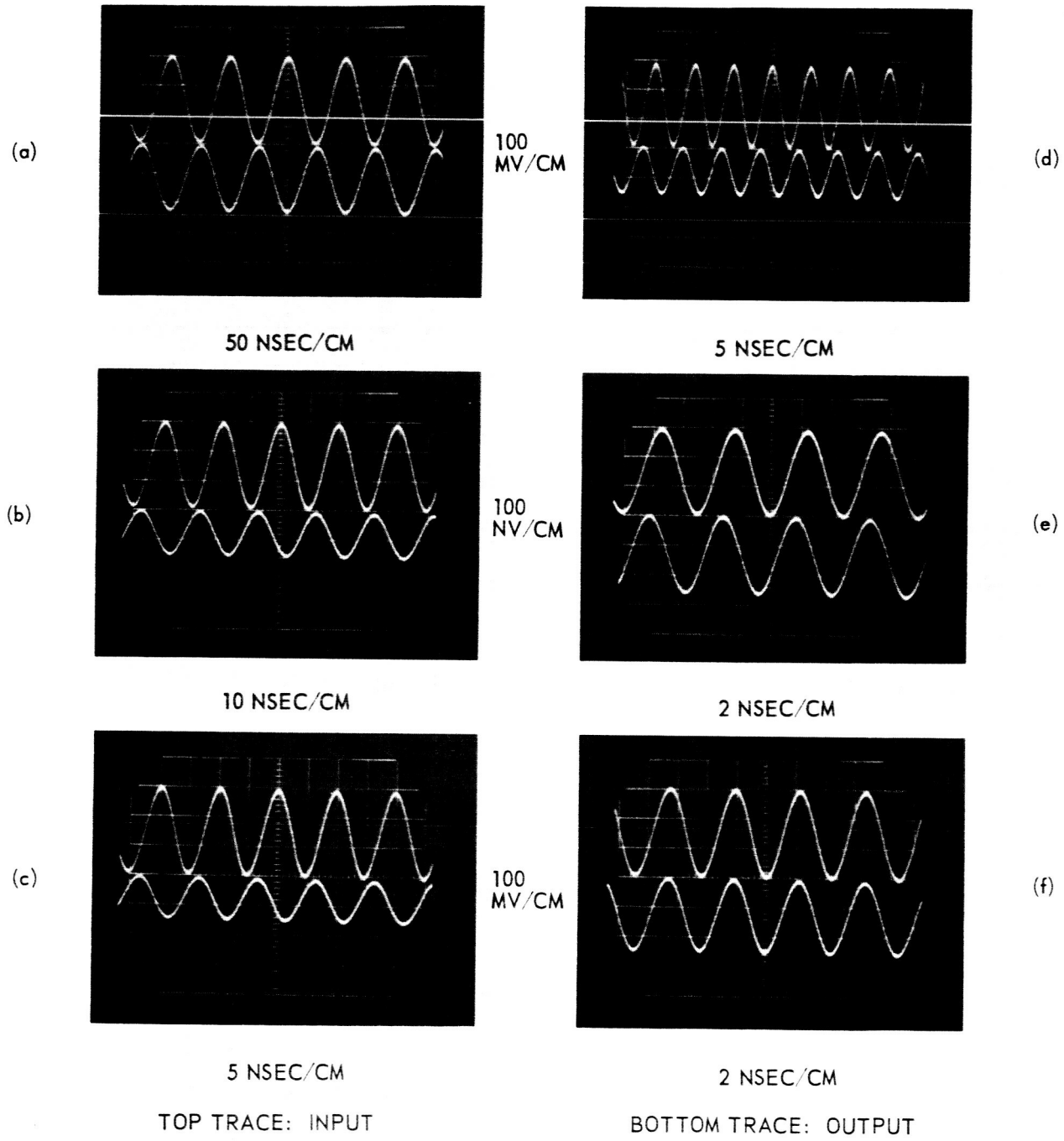


Figure 35. Transformer T3

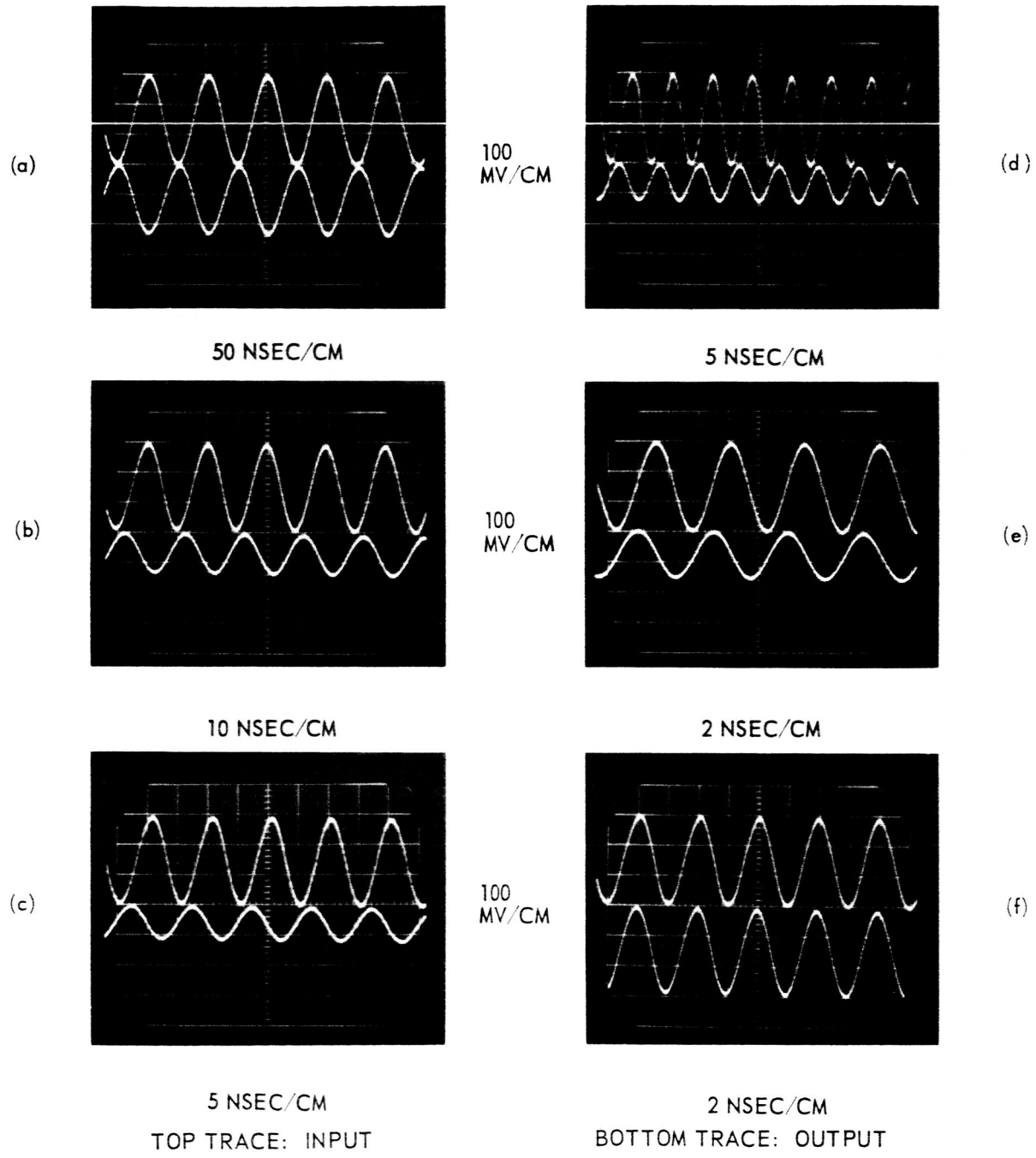


Figure 36. Transformer T4

Transformer T4 is the same as T2 except that two inner turns were not deposited on one coil. This formed a step-up transformer. As shown in table 5 and figure 36, there occurred an increase in the voltage ratio at 10 mc from 0.6 to 0.8. This increase, however, was swamped out at increased frequencies by the overriding capacitive effect.

In the next section calculations are made which show that a poorly coupled transformer can cause a transformer phase shift up to 90°. The shift to 180° is made when the capacitor formed by both coils, with the substrate for a dielectric, begins to affect the operation. This occurs when the frequency reaches a high enough level to have the capacitive reactance low enough to form a shunt path. Prior to this the shift up to 90° is probably caused exclusively by the fact that the transformers are so different from ideal.

7.3 Transformer Calculations

To clarify some of the operational characteristics of the thin-film transformers with ideal transformers, some of the basic transformer theory is presented below. From the basic circuit shown in figure 37, the following equations are derived.[4]

$$j\omega L_1 \bar{I}_1 \pm j\omega M \bar{I}_2 = \bar{V}$$

$$\pm j\omega M \bar{I}_1 + (\bar{Z}_r + j\omega L_2)\, \bar{I}_2 = 0$$

These equations are solved for the impedance as seen from the generator.

$$\frac{\bar{V}}{\bar{I}_1} = \bar{Z} = \frac{\omega^2(M^2 - L_1 L_2) + j\omega L_1 \bar{Z}_r}{\bar{Z}_r + j\omega L_2}$$

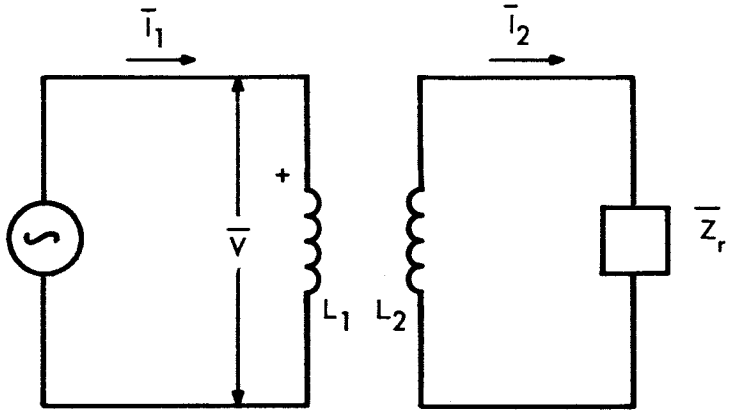


Figure 37. Typical Transformer Circuit

The mutual inductance M between the coils is defined as

$$M = k\,(L_1 L_2)^{1/2}$$

where k is the coupling coefficient. For ideal conditions, when k equals 1 and the coil reactance $j\omega L_2$ is much greater than $\bar{Z}_r$, the reflected impedance equation simplifies to

$$\bar{Z} = \frac{L_1}{L_2}\,\bar{Z}_r$$

Since inductances L_1 and L_2 are proportional to the square of the number of coil turns, this equation can be rewritten

$$\bar{Z} = \left(\frac{N_1}{N_2}\right)^2\,\bar{Z}_r$$

These simplifications do not hold true for the thin-film transformers. The coupling coefficient (k) is less than 1, and $j\omega L_2$ is in the same range as $\bar{Z}_r$. Breaking the basic impedance formula into its real and imaginary parts can help to explain what is actually occurring. For this analysis L_1 is equal to L_2, so that

$$M = k\,(L_1 L_2)^{1/2} = kL$$

Then the impedance equation is organized to find out what happens when ω and/or L approach 0.

$$\bar{Z} = \frac{(\omega L k)^2\,\bar{Z}_r}{\bar{Z}_r^{\,2} + (\omega L)^2} + \frac{\omega L\left[\bar{Z}_r^{\,2} - \omega^2 L\,(k^2 - 1)\right]}{\bar{Z}_r^{\,2} + (\omega L)^2}$$

for

$$k = 1$$

$$\omega \text{ and/or } L \longrightarrow 0$$

$$\bar{Z} \text{ real} \longrightarrow 0$$

$$\bar{Z} \text{ imaginary} \longrightarrow 0$$

Then the impedance equation is reorganized again to find out what happens when ω and/or L approach infinity.

$$\bar{Z} = \frac{k^2 \bar{Z}_r}{\frac{\bar{Z}_r^2}{(\omega L)^2} + 1} + j \frac{\frac{1}{\omega L}\left[\bar{Z}_r^2 - \omega^2 L (k^2 - 1)\right]}{\frac{\bar{Z}_r^2}{(\omega L)^2} + 1}$$

for

$$k = 1$$

$$\omega \text{ and/or } L \longrightarrow \infty$$

$$\bar{Z} \text{ real} \longrightarrow \bar{Z}_r$$

$$\bar{Z} \text{ imaginary} \longrightarrow 0$$

These algebraic gymnastics demonstrate by another approach that when k equals 1 and L_1 equals L_2, and if also ωL is much greater than $\bar{Z}_r$, an ideal transformer with a turns ratio of 1 will be achieved. However, these equations also demonstrate that if k is not equal to 1, an imaginary component will be added and thus the transformer will have an inherent phase shift of its own. This is also true when ωL is not much greater than $\bar{Z}_r$, which explains the particular importance of good coupling. It should be noted that when the imaginary component approaches infinity, the maximum inherent

transformer phase shift can only be 90°. The phase shift back into phase from 180° out of phase in the thin-film transformers is due to the over-riding capacitive effect which occurs when the coils become capacitor plates with the substrate serving as the dielectric. This occurrence is also enhanced by the fact that the current in the adjacent coil turns behaves somewhat as a sheet current. As the frequency and the current density of the conductor edges increase, the coil approaches the characteristics of a sheet of metal just the same as a capacitor plate.

7.4 Conclusions

If transformers are required for the TFPCTS, these thin-film transformers could probably be adapted. The actual requirement would have to be defined before further work would be of any benefit to the program. Shielding of these transformers with thin copper foil did not have any marked effect on their performance, which both made their use seem a little more realistic. and proved that most of the coupling is done through the substrate.

8. HIGH PERMEABILITY MAGNETIC THIN FILMS

8.1 Introduction

The initial investigations concerning the magnetic films in phase A of this contract were research-oriented. The efforts were directed toward the formation of thin-film ferrites by standard deposition techniques (completely in vacuo). The overall goal was the fabrication of thin-film ferrites for use as magnetic planar cores for thin-film inductors.

The deposition and formation of ferrite films have been accomplished by electron beam evaporation of bulk ferrites in a partial pressure of oxygen,[5] postoxidation of vacuum-deposited metals or metal combinations,[6,7] sputtering,[8,9] and pyrolytic chemical reaction.[10,11]

A new method of depositing ferromagnetic films that exhibit various degrees of magnetic structure from Fe_3O_4-B_2O_3 mixture in a vacuum was developed during this contract and has been reported by Hacskaylo.[12] The method of evaporating such mixtures stemmed from the efforts of vacuum-depositing electrically stable rare-earth borosilicate thin-film capacitors from metal boats.[13]

8.2 Film Structure

The method is to mix a small percentage of a stable and low-melting temperature oxide (B_2O_3) with Fe_3O_4 powder. The mixture is deposited from a tungsten boat on substrates at elevated temperatures in vacuums of about $1x10^{-5}$ torr. Standard vacuum deposition techniques are used throughout this investigation.

It was found that films resulting from a Fe_3O_4-B_2O_3 mixture of 95:5 by weight were optimum. A larger ratio of B_2O_3 resulted in films that were

hydroscopic and light in color, whereas a lesser ratio of B_2O_3 resulted in films that were reduced metal (or nearly so). The properties of the films deposited from a 95:5 mixture are reviewed herein.

The films that were deposited on substrates from RT to 520°C did not exhibit diffraction lines. The films that were deposited on the substrates at 200° to 400°C and annealed *in situ* in the vacuum of 1×10^{-5} torr in a temperature range of 550° to 750°C did exhibit various degrees of magnetite. The X-ray diffraction lines of the Fe_3O_4 powder, and of the films annealed for 15 minutes in vacuum at 520°, 650°, and 750°C, and the lines are compared with the ASTM lines shown in figure 38.

Films deposited on SiO-coated copper grids at thicknesses of approximately 50 A at RT were examined in air with an electron microscope. They were found to be amorphous and continuous. The samples were heated *in situ* in the microscope, and the film structure changes were observed as a function of temperature. The films were amorphous to 420°C; but, at 550°C, a high density of crystals formed rapidly. The electron transmission diffraction patterns of the film at 800°C, in general, agree with the X-ray diffraction patterns of ferrite films annealed at 750°C for 15 minutes in the vacuum system.

8.3 Optical Reflectance Spectra

The optical reflectance spectra from 200 to 650 mμ wavelengths were analyzed on a Cary 14 spectrophotometer. The curve is shown in figure 39. The smooth line curve in figure 39 is the reflectance curve of bulk Fe_3O_4 obtained by Vratny and Kokalas.[14] On the same tracing is the reflectance curve obtained from the vacuum-deposited ferrite films and heated to 750°C

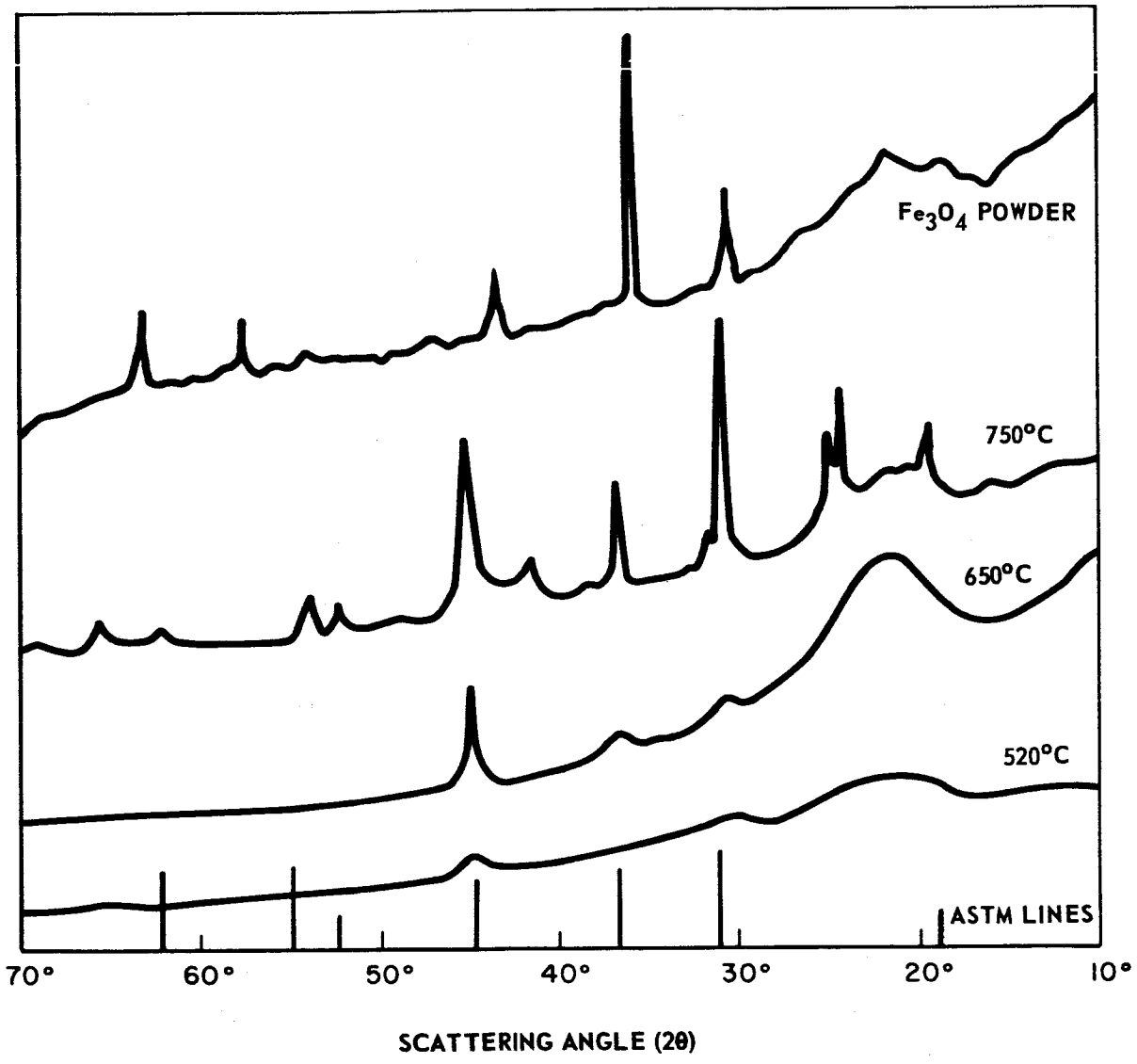
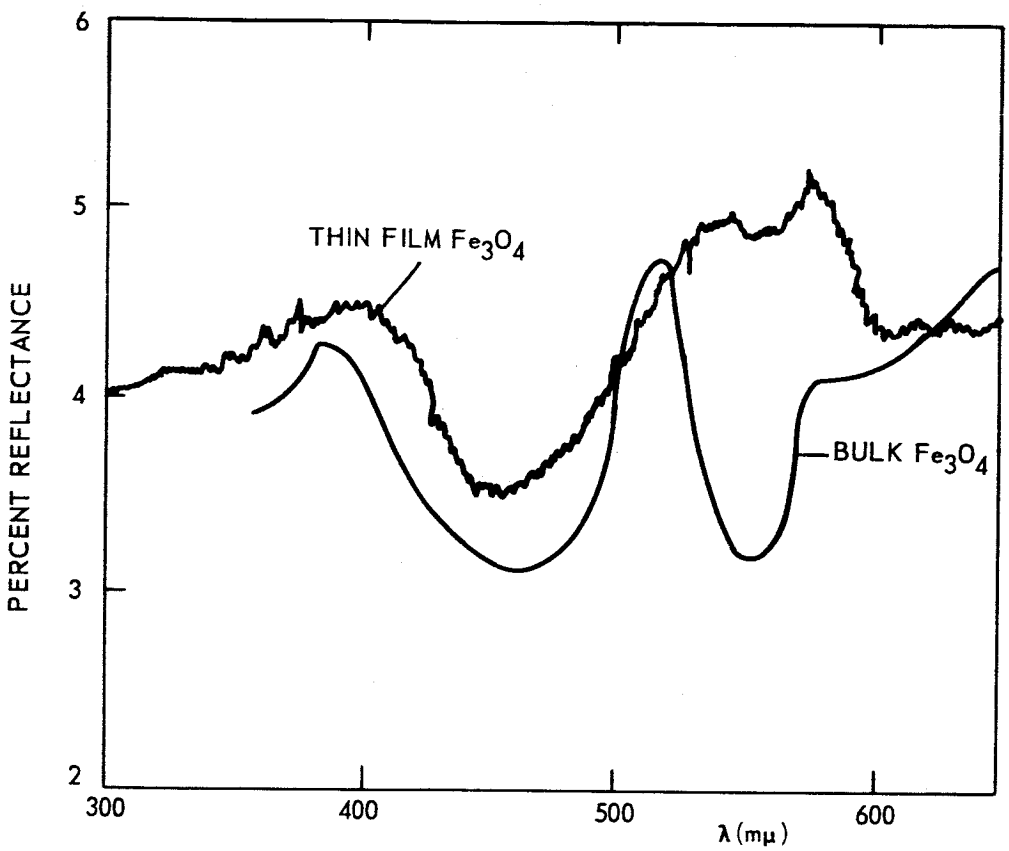


Figure 38. X-Ray Diffraction Patterns of Fe_3O_4 Films at Various Substrate Temperatures



REFLECTION SPECTRA OF Fe_3O_4

Figure 39. Reflectance Spectra of Fe_3O_4

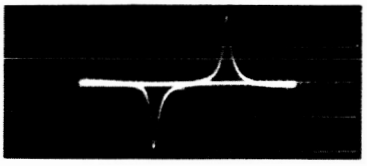
in the vacuum. The bands at 390 and 580 mμ show good agreement. The band at 510 mμ of the bulk sample does not have an exact agreement with the film, but the general agreement of the bulk and film optical properties indicates that the film structure is similar to the bulk material.

8.4 Electrical Properties

The electrical properties of the vacuum-deposited films of the Fe_3O_4-B_2O_3 mixtures were briefly investigated, and the resistance of the films cannot be related to the film composition and structure at this time.

8.5 Magnetic Properties

The magnetic dB/dt peaks (unintegrated signals) and the B-H loops (integrated signals) were measured by a modified Helmholtz drive coil with a figure 8 sense coil.[15] The field, in oersteds, was linear with drive coil current to the maximum drive field of 60 oersteds. The dB/dt peaks at 600 cps and the integrated signal are shown in figure 40. The switching field strength is 2.7 oersteds. The inductance, or the value of B of the B-H loops, cannot be measured directly, since the vertical response to a voltage signal corresponding to the magnetic induction is not readily calculable. However, it is possible to calibrate the vertical signal -- the magnetic induction in gauss -- by inserting a known film value of a standard ferromagnetic film. According to Neugebauer,[16] the $4\pi M_s$ (saturation magnetization) of the nickel in film is the same as in bulk form. The saturization magnetization was measured to be approximately 6000 gauss by comparing the B-H curves with that of nickel film and foil. This value is comparable to the value for magnetite; however, the coercive field of these films is several magnitudes less than that of the bulk magnetite.



(a)

(b)

Figure 40. dB/dt Peaks (a) and Integrated B-H Loop (b) of Ferrite Films

The unintegrated switching pulses can be used as an accurate method of determining the easy axes of the films.17 The plot of the magnitude (in arbitrary units) of the peaks as a function of rotation angle is shown in figure 41. The inserts are oscilloscopic traces of the dB/dt peaks at angular positions of 0°, 45°, 60°, 90°, and 120°. The cusp axes are experimentally within $\pm 2.5^{\circ}$ of a hexagonal axis orientated so that one of the axes is parallel to the strongest dB/dt signal. The sixfold angular magnetic anisotropy phenomenon for the films reported here was consistent, regardless of film geometrics at substrate temperatures below $300^{\circ}C$.

A brief discussion by Prutton18 concerning the Kaya effect (the inclusion of ordered domains in a disordered matrix) indicates that the observed magnetic anisotropy, high saturation magnetization, and low coercivities could be due to microscopic inclusions of cobalt and nickel as well as elemental iron. Spectrographic analyses of the films deposited on carbon rods showed that B, Co, and Ni as well as Al, Co, Cr, and Mn were impurities present to a total concentration of approximately 1%. However, elemental iron was detected in the evaporated films, and the concentration ranged from 100 ppm to 0.1% as determined by chemical wet analyses. In this specific case, the hexagonal magnetic anisotropy could be associated with the microscopic domains of the metal cations.

8.6 Inductor Core Evaluation and Conduction

The induction of thin-film inductors was not improved by the deposition of the ferrites on the inductors. The dielectric loss and film conductivity are both high, agreeing with magnetitic materials. Thus, the formation of high resistivity ferrite films of mixed cation oxides should be the next phase of investigation.

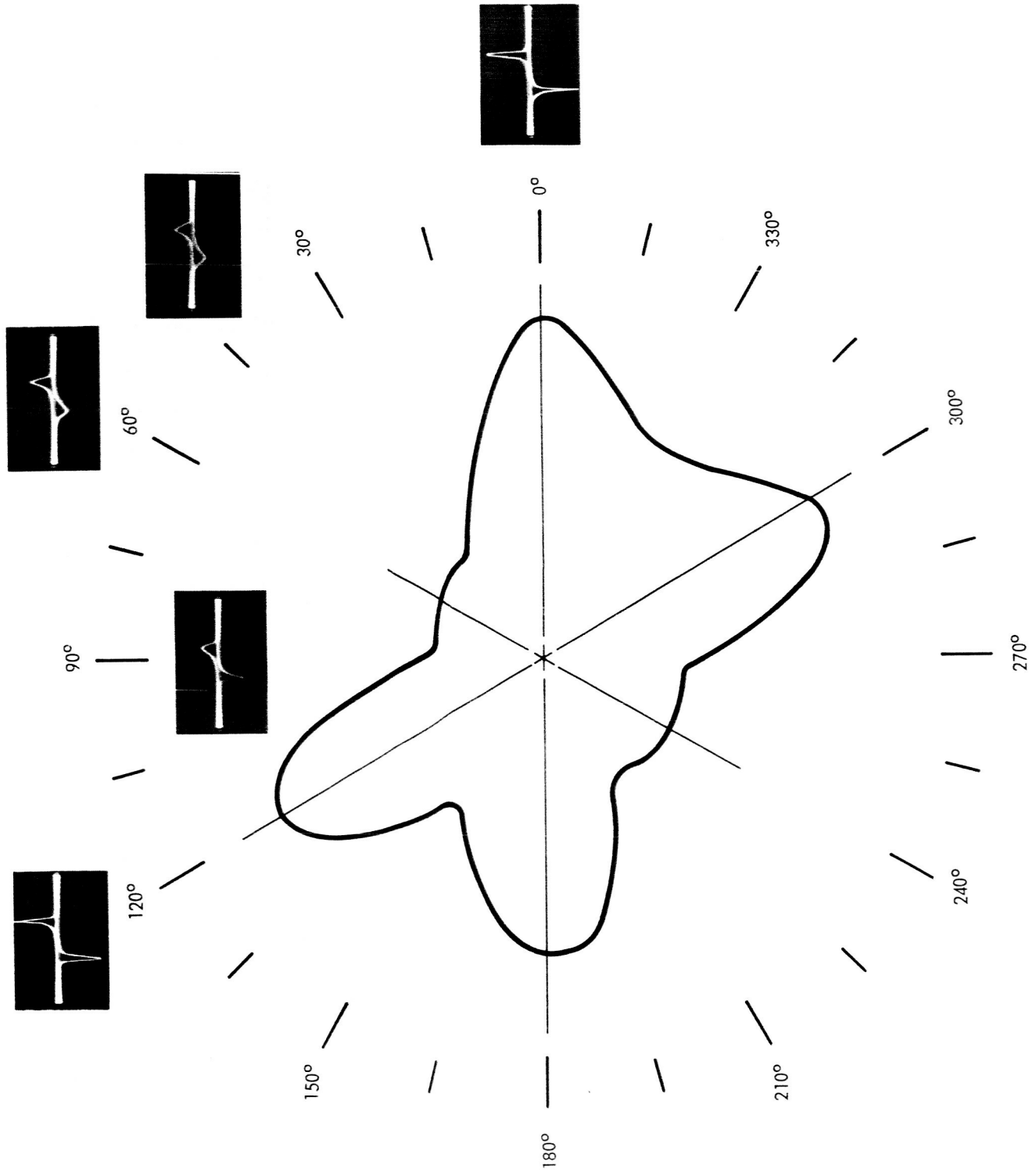


Figure 41. Plot of Average Amplitude of dB/dt Peaks as Film Is Rotated in Magnetic Drive Field

9. CIRCUIT DESIGN CONSIDERATIONS

During Phase A, Melpar has supported a parallel effort to develop the circuits required to initiate Phase B. Table 6 gives the estimate of the number of circuits which can be completely fabricated in thin-film form.

9.1 Circuit types

Circuits that have been breadboarded in discrete form include:

a. VCO's.

b. VCO filters.

c. Audio amplifiers.

d. I-F amplifier.

e. R-F amplifiers.

f. R-F oscillators.

g. Frequency multipliers.

h. Mixers.

In all cases the circuits were designed with components that have similar characteristics to thin-film components. The breadboard was designed in modular form so that thin-film substrates can be substituted for the discrete component modules.

9.2 Circuit Discussion

Reports on the circuit layout and performance will become part of the Phase B effort. Except for the transmitter output power, the circuits meet the specifications of the contract work statement. The output power cannot be attained at the present time with field effect transistors. Conventional transistors may have to be used for this purpose.

TABLE 6

COMPONENT ESTIMATES FOR TFPCTS

	Transistors	Coils	R	C	Diodes	Other
Duplex transmitter	4 (HF)	5	5	14	-	1 crystal
VCO's (7)	14 (LF)		42	14	14	-
VCO filters	-	-	18	18	-	-
VCO adder amplifier	2 (LF)	-	8	2	-	-
2.3-kc filter	2 (LF)	-	5	5	-	-
VOX duplex	6 (LF)	-	18	6	1	-
Duplex receiver	4 (HF)	5	5	14	-	1
Simplex receiver	4 (HP)	5	5	14	-	1
Diplexer	-	5	5	-	-	-
I-F duplex	15 (LF)	-	45	28	3	-
I-F simplex	15 (LF)	-	45	28	3	-
Audio duplex	4 (LF)	-	12	9	-	-
Audio simplex	4 (LF)	-	12	9	-	-
Simplex transmitter	4 (HF)	5	5	14	-	1
2.3-kc filter	2 (LF)	-	5	5	-	-
VOX simplex	6 (LF)	-	18	6	1	-
Power supply	4 (High current)		15	10	4	-
	6 (Low power)				1 reference	
VCO regulators					7 reference	
Totals	16 HF 76 LF	25	268	196	26 diodes	4
	4 high current		(2 large C)		8 reference	

A second problem area is the receiver input for large signals. The specifications require that the receiver should be capable of operation at a 1.4-volt peak-to-peak input signal. At this level the r-f amplifier is saturated and introduces considerable distortion. This situation can be corrected by using AGC voltage to tune the input slightly off the center frequency. Since the transistor input capacitance is a function of the applied voltage, the AGC voltage can be applied to the gate in a conventional manner.

9.3 Conclusions

At the present time, it appears that more than 90% of the components necessary for the TFPCTC (listed in table 6) can be fabricated in thin-film form.

10. CONCLUSIONS

It is difficult to draw finalized conclusions from this continuing research program. Certain areas, such as "High Frequency Substrate Evaluation," "Dielectric Investigation," and "Inductors," can be concluded as having been suitable for use at frequencies up to 300 mc. Although a chemical ferrite was vacuum-deposited, it is beyond the scope of this contract to develop it until it is suitable for circuit use. The development of a vacuum-deposited thin-film metal-semiconductor diode, similar in operation to the metal-semiconductor junctions formed through solid-state technology for use as gigacycle/second varactors, has been invaluable to this program. Since these diodes were vacuum-deposited in transistor configuration and transistor action was obtained, the potential for usable thin-film junction transistors exists in the near future.

The research expended on "High Frequency Thin-Film Triodes," to improve these devices for high-frequency use, not only evolved a TFT with an order of magnitude of frequency performance 30 mc higher than previous TFT's, but also helped to better define the operating characteristics of the field effect mechanisms which will help in solving any device stability and lifetime problems. Also, the combination of all the necessary parameters into a device for operation at 300 mc may be realized in the near future, hopefully in time to be included in the TFPCTS.

The conclusion for phase A is best summed up in section 9 of this report. At the present time, it appears from the breadboarded circuits for the TFPCTS that more than 90% of the components can be fabricated in thin-film form. The circuit concept was conceived and designed to be the best suited for, and also to obtain the maximum benefits of, the many advantages available in monotronic circuits.

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